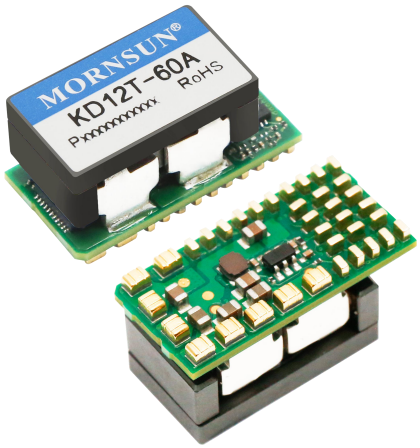
非隔离稳压单路 60A/双路 30A 输出，POL 数字模块电源



专利保护 RoHS

- 输入欠压、输出欠压/过压保护
- 输出过流保护
- 过温保护
- 黑匣子故障记录

产品特点

- 小体积封装：25.4 x 12.7 x 12.96 mm
- 可灵活配置单路输出/双路输出
- 宽输入电压范围：7.5-14.4VDC
- 宽输出电压范围：0.6-4.5V
- 极小的输出电压偏差：±10mV
- 极低的输出纹波和噪声：7mVp-p
- 最大输出电流可高达单路 60A/双路 30A
- 效率可高达 92%
- 最大可支持两模块并联，电流共享提升至 120A
- 具有极小的负载动态变化：30mV
- 宽工作温度范围：-40℃ to 85℃
- 可通过 PMBus 进行配置和监控
- 固定开关频率，并具备同步外部时钟功能
- 具备远端补偿功能
- 具备输出跟踪和电源排序功能

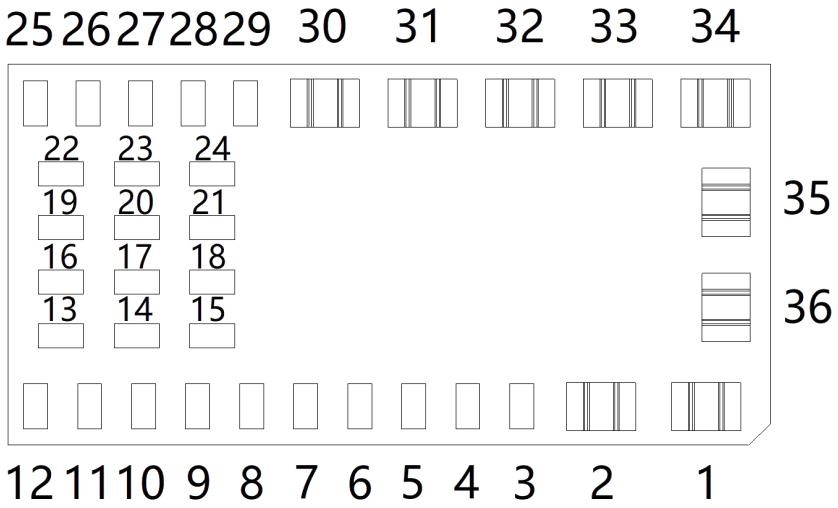
KD12T-60A 数字模块是非隔离 DC-DC 转换器，可提供高达 60A 单路/30A 双路的输出电流。该模块可满足 7.5 至 14.4VDC 的输入电压范围，并提供可调的精确的 0.6 至 4.5VDC 的输出电压，其输出电压可通过外部电阻分压或 PMBus 命令进行配置。该模块的功能还包括 PMBus 数字协议，远程 CNTL，Power Good，过流，欠压，过压和过温保护。模块内部还包括一个实时补偿环路，用于优化动态响应以匹配负载跳变时的变化。该模块广泛应用于通信、计算机网络、电力分布式架构、工作站、服务器、局域网/广域网等领域，为 FPGA、DSP、ASIC 等高速芯片提供大电流瞬态响应快的稳定电压。

选型表

认证	产品型号	输入电压（VDC）	输出		输出电压偏差	输出电压纹波&噪声
		标称值（范围值）	电压（VDC）（范围值）	输出电流（A）最大值	（mV）最大值	（mVp-p）典型值
--	KD12T-60A	12（7.5-14.4）	0.6-4.5	60	±10	7

目录

引脚说明

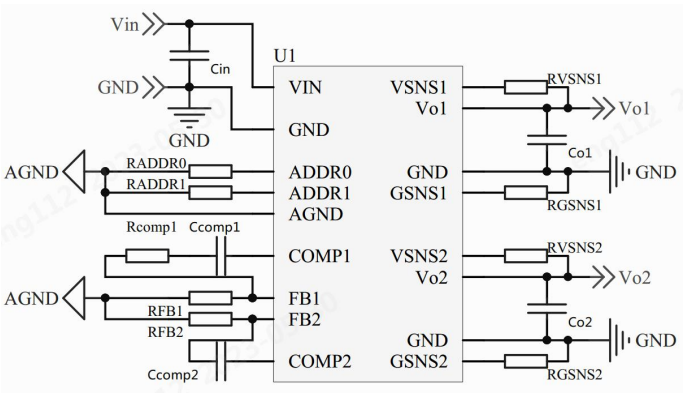


引脚布局的底部视图

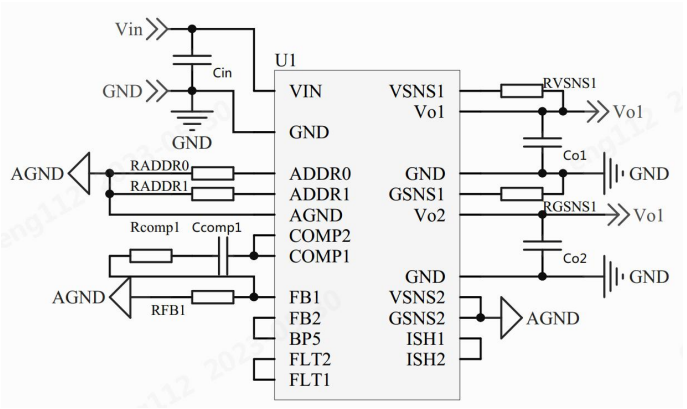
引脚	符号	类型	功能
1, 36	VIN	Power	输入电压
2	GND	Power	输入电源地
3	PG2	O	通道 2 的指示输出电压是否良好的开漏引脚，该引脚在从机时被内部拉至地。
4	PG1	O	通道 1 的指示输出电压是否良好的开漏引脚，该引脚在从机时被内部拉至地。
5	CNTL2	I	开启/关断通道 2 的控制信号输入引脚。当该引脚悬空时，一个内部 6uA 的电流会将 CNTL 上拉至 BP5
6	CNTL1	I	开启/关断通道 1 的控制信号输入引脚。当该引脚悬空时，一个内部 6uA 的电流会将 CNTL 上拉至 BP5
7	SYNC	I/O	用于使用外部时钟的同步时钟引脚。外部的 SYNC 同步信号在单相、两相和四相的时候必须是所需开关频率的四倍，在三相的时候必须为 3 倍。
8	NC	/	无功能引脚
9	ADDR1	I	高阶地址位引脚，接电阻至地，详见 PMBus 地址配置说明
10	PMBCLK	I	PMBus 时钟引脚
11	PMBDATA	I/O	PMBus 数据引脚
12	SMBALERT	O	PMBus ALERT 引脚
13	AGND	/	数字地
14	COMP1	O	通道 1 的误差放大器输出
15	FLT1	I/O	通道 1 的故障信号引脚
16	NC	/	无功能引脚
17	PHSET	I/O	多相模式下的相位设置引脚
18	ISH1	I	通道 1 的电流共享信号引脚
19	BP5	O	内部稳压器的输出旁路引脚
20	ADDR0	I	低阶地址位引脚，接电阻至地，详见 PMBus 地址配置说明
21	ISH2	I	通道 2 的电流共享信号引脚
22	FB2	I	通道 2 的误差放大器的输入。在正常工作下，该引脚电压等于内部基准电压。设置从机时需将该引脚连接至 BP5
23	FLT2	I/O	通道 2 的故障信号引脚
24	COMP2	O	通道 2 的误差放大器输出
25	VSENS2	I	通道 2 的输出电压远端检测正信号引脚
26	GSENS2	I	通道 2 的输出电压远端检测负信号引脚
27	FB1	I	通道 1 的误差放大器的输入。在正常工作下，该引脚电压等于内部基准电压。

28	GSENS1	I	通道 1 的输出电压远端检测负信号引脚
29	VSENS1	I	通道 1 的输出电压远端检测正信号引脚
30, 31	VO2	Power	通道 2 的电压输出
32	GND	Power	通道 2 的电压输出地
33, 34	VO1	Power	通道 1 的电压输出
35	GND	Power	通道 1 的电压输出地

典型应用电路



双路输出

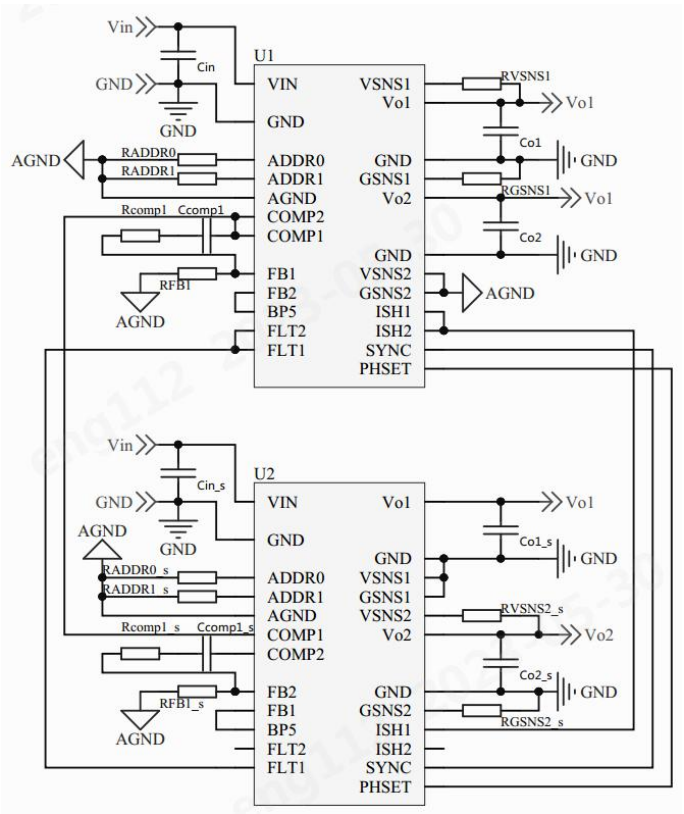


两相应用/单路输出

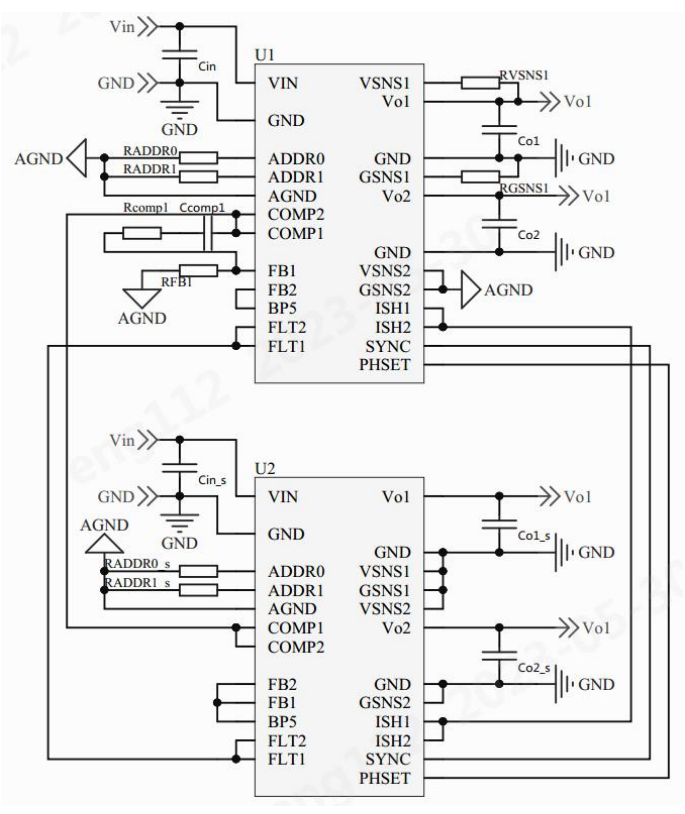
引脚	双路输出	两相应用/单路输出
SYNC	悬空或连接至外部时钟	悬空或连接至外部时钟
PHSET	悬空	悬空
FB1	通道 1 的误差放大器输入	通道 1 的误差放大器输入
FB2	通道 2 的误差放大器输入	连接至 BP5
COMP1	通道 1 的误差放大器输出	通道 1 的误差放大器输出，连接至 COMP 总线
COMP2	通道 2 的误差放大器输出	连接至 COMP 总线
ISH1	悬空	连接至 ISH 总线
ISH2	悬空	连接至 ISH 总线
FLT1	通道 1 的故障信号	连接至 FLT 总线
FLT2	通道 2 的故障信号	连接至 FLT 总线
PG1	通道 1 的 POWER GOOD 信号，通过上拉电阻连接至 BP5	两相应用的输出电压的 POWER GOOD 信号，通过上拉电阻连接至 BP5
PG2	通道 2 的 POWER GOOD 信号，通过上拉电阻连接至 BP5	悬空或连接至地
VSENS1	通道 1 的输出电压远端补偿正信号	两相应用的输出电压远端补偿正信号
GSENS1	通道 1 的输出电压远端补偿负信号	两相应用的输出电压远端补偿负信号
VSENS2	通道 2 的输出电压远端补偿正信号	连接到地或输出电压
GSENS2	通道 2 的输出电压远端补偿负信号	连接到地
CNTL1	通道 1 的远程控制信号	两相应用的远程控制信号
CNTL2	通道 2 的远程控制信号	悬空

注：两相应用时 Ccomp1 推荐为 470pF。

典型应用电路



三相应用



四相应用

模块	引脚	三相应用	四相应用
主机 /U1	SYNC	连接至 SYNC 总线	连接至 SYNC 总线
	PHSET	连接至 PHSET 总线	连接至 PHSET 总线
	FB1	模块 1 的通道 1 的误差放大器输入	模块 1 的通道 1 的误差放大器输入
	FB2	连接至模块 1 的 BP5 引脚	连接至模块 1 的 BP5 引脚
	COMP1	模块 1 的通道 1 的误差放大器输出，连接至 COMP 总线	模块 1 的通道 1 的误差放大器输出，连接至 COMP 总线
	COMP2	连接至 COMP 总线	连接至 COMP 总线
	ISH1	连接至 ISH 总线	连接至 ISH 总线
	ISH2	连接至 ISH 总线	连接至 ISH 总线
	FLT1	连接至 FLT 总线	连接至 FLT 总线
	FLT2	连接至 FLT 总线	连接至 FLT 总线
	PG1	三相应用的的 POWER GOOD 信号,通过上拉电阻连接至 BP5	四相应用的压的 POWER GOOD 信号，通过上拉电阻连接至 BP5
	PG2	悬空或连接至地	悬空或连接至地
	VSENS1	三相应用的输出电压远端补偿正信号	四相应用的输出电压远端补偿正信号
	GSENS1	三相应用的输出电压远端补偿负信号	四相应用的输出电压远端补偿负信号
	VSENS2	连接到地或输出电压	连接到地或输出电压
	GSENS2	连接到地	连接到地
	CNTL1	三相应用的远程控制信号	四相应用的远程控制信号
	CNTL2	悬空	悬空

注：

1. 三相应用和四相应用下，Ccomp1 推荐为 1000pF

2. 四相应用下输入电压范围为 10-14.4V

典型应用电路

模块	引脚	三相应用	四相应用
从机 /U2	SYNC	连接至 SYNC 总线	连接至 SYNC 总线
	PHSET	连接至 PHSET 总线	连接至 PHSET 总线
	FB1	连接至模块 2 的 BP5	连接至模块 2 的 BP5
	FB2	模块 2 的通道 2 的误差放大器输入	连接至模块 2 的 BP5
	COMP1	连接至 COMP 总线	连接至 COMP 总线
	COMP2	模块 2 的通道 2 的误差放大器输出	连接至 COMP 总线
	ISH1	连接至 ISH 总线	连接至 ISH 总线
	ISH2	悬空	连接至 ISH 总线
	FLT1	连接至 FLT 总线	连接至 FLT 总线
	FLT2	模块 2 的通道 2 的故障信号	连接至 FLT 总线
	PG1	悬空/连接至地	悬空/连接至地
	PG2	模块 2 的通道 2 的输出电压的 POWER GOOD 信号，通过上拉电阻连接至 BP5	悬空/连接至地
	VSENS1	连接至地或输出电压	连接至地或输出电压
	GSENS1	连接至地	连接至地
	VSENS2	模块 2 的通道 2 的输出电压远端补偿正信号	连接至地或输出电压
	GSENS2	模块 2 的通道 2 的输出电压远端补偿负信号	连接至地
	CNTL1	连接至模块 1 的 CNTL1 引脚	连接至模块 1 的 CNTL1 引脚
	CNTL2	模块 2 的通道 2 的远程控制信号	悬空

注：

1. 三相应用和四相应用下，Ccomp1 推荐为 1000pF

2. 四相应用下输入电压范围为 10-14.4V

极限额定值

		最小值	最大值	单位
电压	Vin	-0.3	16	V
	BP5、FB、PG、CNTL、COMP、FLT	-0.3	7	V
	GSNS、VSNS、PMBDATA、SMBALERT、PMBCLK、SYNC、ISH、PHSET	-0.3	5.5	V
	ADDR	-0.3	3.6	V
温度	工作温度 （详见温度降额曲线）	-40	85	℃
	存储温度	-55	125	℃
湿度	存储湿度（无凝结）	5	95	%RH
海拔高度		--	2000	m
回流焊温度	IPC/JEDEC J-STD-020D.1.	峰值温度 Tc≤245℃,217℃以上时间最大为 60 s		
潮敏等级	IPC/JEDEC J-STD-020D.1	MSL 3		
污染等级		PD 3		
振动		IEC/EN61373 - Category 1, Grade B		

注：
超出极限额定值可能会对模块造成永久性损坏，长时间暴露在极限额定值下会影响模块的可靠性。另外这些只是应力等级，并不意味着模块可以在极限额定值条件范围内进行功能操作。

配置文件

本产品采用数字控制电路设计，数字控制电路使用一个配置文件决定产品的功能和性能。除非另有说明，电气规格表显示的均为标准配置文件下的功能和性能规格值。标准配置文件可以适应大多数应用需求。在特定的应用中，可以更改标准配置文件以优化性能。注意，若需使用多相并联时需要更改配置文件。

通用电气规格

以下部分规格与产品的数字控制相关，可通过 PMBus 配置的参数命令已用大写字母标注。

若无特殊说明，以下规格的工作温度范围为-40 至+85℃，输入电压为 7.5 至 14.4 V，工作频率为 430kHz；以下规格的典型值的工作条件为工作温度+25℃，输入电压 12.0 V，满载输出；另外输出电压需在引脚上测量，数字控制为标准配置文件。

规格		条件	最小值	典型值	最大值	单位
频率和时钟同步						
f	开关频率	默认值	--	430	--	kHz
	开关频率范围 (1)	SYNC 引脚输入	200	--	1500	kHz
	SYNC 信号高电平阈值 (2)		2	--	--	V
	SYNC 信号低电平阈值 (2)		--	--	0.8	V
	最小 SYNC 脉冲宽度		--	100	--	ns
（1）更改开关频率会影响模块性能，更改前请与 FAE 确认。 （2）外部同步时钟引脚信号必须是占空比为 50%的方形波形。						
初始化时间和软启动						
T_{INI}	初始化时间	BP5 电压建立后	--	1	--	ms
t_{ss}	软启动时间 (1)	默认值	--	2.7	--	ms
	软启动时间可配置范围		0.6	--	9	ms
	软启动时间配置精度		-15	--	15	%
（1）软启动时间是内部参考电压从 0V 上升到 600mV 的时间。						
PGOOD						
V_{FBPGH}	FB PGOOD 高电平阈值	默认值	--	642	--	mV
V_{FBPGL}	FB PGOOD 低电平阈值	默认值	--	558	--	mV
$V_{PG\ (acc)}$	PGOOD 阈值配置精度		-4	--	4	%
$V_{PG\ (hyst)}$	FB PGOOD 回差电压		15	28	45	mV
R_{PGOOD}	PGOOD 内部下拉电阻	V_{FB}=0V, I_{PGOOD}=5mA	--	50	--	Ω
$I_{PGOOD\ (lk)}$	PGOOD 引脚漏电流	V_{FB} = 600 mV, V_{PGOOD} = 5 V	--	--	20	uA
$t_{PGDELAY}$	PGOOD 延迟时间	默认值（软启动完成后）	--	2	--	ms
VSNS/GSNS						
远程补偿范围			--	--	0.5	%Vo
输入欠压保护						
$V_{IN\ (on)}$	输入欠压开启电压 (1)	默认值	--	6.25	--	V
$V_{IN\ (off)}$	输入欠压关断电压 (1)	默认值	--	6	--	V
$V_{INON\ (rng)}$	输入欠压开启电压可配置范围		4.25	--	14	V
$V_{INOFF\ (rng)}$	输入欠压关断电压可配置范围		4	--	13.75	V
（1） 输入欠压回差至少设置在 150mV 以上						
输出过压/欠压保护						
V_{FBOV}	FB 过压阈值 (1)	默认值	--	800	--	mV
V_{FBUV}	FB 欠压阈值	默认值	--	528	--	mV
$V_{UVOV\ (acc)}$	FB 过压/欠压阈值配置精度		-4	--	4	%
（1） FB 基准电压为 600mV，FB 电压达到 600mV 后，产品关断驱动，但不进入过压保护状态（锁存关断）						
电流限制						

$t_{OFF\ (oc)}$	打嗝时间	配置为打嗝模式		$7 \times t_{ss}$		ms
$I_{OC\ (flt)}$	输出过流故障阈值	默认值	--	50	--	A
		可配置范围	3	--	50	
$I_{OC\ (warn)}$	输出过流警告阈值	默认值	--	49	--	A
		可配置范围	2	--	49	
$I_{OC\ (acc)}$	输出过流故障阈值配置精度	IOUT = 40 A, IOUT_CAL_GAIN = 0.503 mΩ	-10	--	10	%
	输出过流警告阈值配置精度	IOUT = 37 A, IOUT_CAL_GAIN = 0.503 mΩ	-10	--	10	
短路保护		默认值	锁存，重启恢复			
温度检测和过温关断						
T_{SD_P1}	P1 关断结温 (1)		--	160	--	℃
T_{HYST_P1}	P1 关断回差 (1)		--	20	--	℃
$T_{SNS\ (acc)\ \_P3/P4}$	P3/P4 温度检测精度 (1)	-40℃ ≤$T_{P3/P4}$≤ 125℃	-3	--	3	℃
$T_{OT\ (flt)\ \_P3/P4}$	P3/P4 过温故障阈值 (1)	默认值	--	165	--	℃
	P3/P4 过温故障阈值配置范围 (1)		120	--	165	℃
$T_{OT\ (warn)\ \_P3/P4}$	P3/P4 过温警告阈值 (1)	默认值	--	140	--	℃
	P3/P4 过温警告阈值配置范围 (1)		100	--	140	℃
$T_{OT\ (step)\ \_P3/P4}$	P3/P4 过温警告/故障配置步进 (1)		--	1	--	℃
$T_{OT\ (hys)\ \_P3/P4}$	P3/P4 过温警告/故障回差 (1)		--	20	--	℃
（1） P1，P2，P3，P4 在以下产品工作温度描述中定义。						
测量系统						
$M_{VOUT\ (rng)}$	输出电压测量范围		0.6	--	4.5	V
$M_{VOUT\ (acc)}$	输出电压测量精度 (2)	V_0 = 1V，0℃≤T_{P1}≤125℃	-0.8	--	0.8	%
$M_{IOUT\ (rng)}$	输出电流测量范围 (1)		0	--	50	A
$M_{IOUT\ (acc)}$	输出电流测量精度 (2)	IOUT≥20 A，IOUT_CAL_GAIN = 0.503 mΩ，0℃≤T_{P1}≤125℃	-640	--	640	mA
（1）实际测量范围限制于 IOUT_CAL_GAIN 指令，详见 IOUT_CAL_GAIN （38h） 环节 （2）在应用条件下的性能验证						
CNTL						
V_{CNTL-H}	输入高电平		2.1	--	5	V
V_{CNTL-H}	输入低电平		0	--	0.5	V
P_{CNTL}	输入待机功耗	CNTL 引脚关断	--	0.55	--	W
$t_{ON\ (dly)}$	开启延迟时间	默认值	--	0	--	ms
$t_{OFF\ (dly)}$	关断延迟时间	默认值	--	0	--	ms
PMBus 交互						
V_{IH}	高电平输入电压，CLK，DATA		2.1	--	--	V
V_{IL}	低电平输入电压，CLK，		--	--	0.8	V

	DATA					
I_{IH}	高电平输入电流，CLK，DATA，CNTL	引脚电压=3.3 V	-10	--	10	uA
I_{IL}	低电平输入电流，CLK，DATA，CNTL	引脚电压=0 V	-10	--	10	uA
V_{OL}	低电平输出电压，DATA，SMBALRT		--	--	0.4	V
I_{OH}	高电平漏电流，DATA，SMBALRT		0	--	10	uA
I_{OL}	低电平漏电流，DATA，SMBALRT		4	--	--	mA
$C_{PIN-OUT}$	引脚电容，CLK，DATA		--	--	1	pF
f_{PMB}	PMBus 工作频率范围	从机	10	--	400	kHz
t_{BUF}	从 START 到 STOP 的总线空闲时间		1.3	--	--	us
$t_{HD:STA}$	重启 START 后的保持时间		0.6	--	--	
$t_{SU:STA}$	重启 START 设置时间		0.6	--	--	
$t_{SU:STO}$	STOP 设置时间		0.6	--	--	
$t_{HD:DAT}$	数据保持时间	接受模式	0	--	--	ns
		传送模式	300	--	--	
$t_{SU:DAT}$	数据设置时间		100	--	--	
$t_{TIMEOUT}$	错误信号/检测		25	--	35	ms
$t_{LOW:MEXT}$	主机累计时钟拓展时间		--	--	10	ms
$t_{LOW:SEXT}$	从机累计时钟拓展时间		--	--	25	ms
t_{LOW}	时钟低时间		1.3	--	--	us
t_{HIGH}	时钟高时间		0.6	--	--	us
t_{FALL}	CLK/DATA 下降时间		--	--	300	ns
t_{RISE}	CLK/DATA 上升时间		--	--	300	ns
$t_{RETENTION}$	配置参数的保留时间	T_{P1} = 25℃	100	--	--	Year
Write_cycles	非易失性擦除/写入周期数	T_{P1} = 25℃	20	--	--	K cycle
外置电容						
C_{OUT-EX}	外置电容	ESR ≥ 0.15 mΩ	330	--	560	uF
		ESR ≥ 10 mΩ	660	--	15000	uf
MTBF						
MTBF			--	6015801	--	Hours
物理机械特性						
重量			--	12	--	g
尺寸			25.4 x 12.7 x 12.96 mm			
冷却方式			空气冷却或强制风冷			

产品电气特性（双路输出）

以下部分规格与产品的数字控制相关，可用于可配置参数的 PMBus 命令已用大写字母标注。

若无特殊说明，以下规格的工作温度范围为-40 至+85℃，输入电压为 7.5 至 14.4 V，频率为 430KHz；以下规格的典型值的工作条件为工作温度 +25℃，输入电压 12.0 V，满载输出；另外输出电压需在引脚上测量，数字控制为标准配置文件，仅使能一路输出。

另外需求外接 C_{IN} = 2x470 uF/10 mΩ OS-CON + 8 x 10 uF 陶瓷电容，C_{OUT} =4 x 330 uF/10 mΩ Polymer + 10 x 100 uF 陶瓷电容，如典型应用电路图。

规格		条件	最小值	典型值	最大值	单位
输入电压						
V_{in}	输入电压		7.5	12	14.4	V
	输入电压上升时间	单调上升	--	--	10	V/ms
输出电压						
V_o	输出电压可调范围	分压电阻配置	0.6	--	4.5	V
		分压电阻 / PMBus 配置	0.54	--	4.5	V
	输出电压设置精度		--	±0.025	--	$\%V_o$
	输出电压精度/偏差	1.0V≤Vo≤4.5V	-1	--	+1	$\%V_o$
		Vo<1.0V	-10	--	10	mV
	线性调整率	Vo = 0.6 V	--	1	--	mV
		Vo = 1.0 V	--	1	--	
		Vo = 1.8 V	--	2	--	
		Vo = 2.5 V	--	3	--	
		Vo = 3.3 V	--	3	--	
		Vo = 4.5 V	--	3	--	
	负载调整率	Vo = 0.6 V	--	1	--	
		Vo = 1.0 V	--	1	--	
		Vo = 1.8 V	--	2	--	
		Vo = 2.5 V	--	2	--	
		Vo = 3.3 V	--	2	--	
		Vo = 4.5 V	--	2	--	
V_{o-ac}	输出纹波&噪声（20MHz 带宽下）	Vo = 0.6 V	--	7	--	mVp-p
		Vo = 1.0 V	--	8	--	
		Vo = 1.8 V	--	12	--	
		Vo = 2.5 V	--	14	--	
		Vo = 3.3 V	--	16	--	
		Vo = 4.5 V	--	19	--	
温度漂移系数		工作温度范围-40℃ to +85℃	--	±0.2	--	%/℃
瞬态响应偏差		标称输入电压，50%负载跳变	--	30	--	mV
瞬态恢复时间			--	1	--	us
输入电流						
$I_{in-no\ load}$	输入空载电流	Vo = 0.6 Vdc	--	80	--	mA
		Vo = 4.5 Vdc	--	150	--	mA
I^2t	瞬时冲击电流		--	--	1	A^2s
输出电流						
I_o	输出电流（每路）	Vo = 0.6 V	0	--	30	A
		Vo = 1.0 V	0	--	30	A

		Vo = 1.8 V	0	--	30	A
		Vo = 2.5 V	0	--	30	A
		Vo = 3.3 V	0	--	27	A
		Vo = 4.5 V	0	--	20	A
I_{lim}	输出电流限制阈值（每路）	OCP 阈值设置为 50 A	--	50	--	A
效率						
η	效率 max I_o	Vo = 0.6 V	--	82	--	%
		Vo = 1.0 V	--	86	--	
		Vo = 1.8 V	--	90	--	
		Vo = 2.5 V	--	91	--	
		Vo = 3.3 V	--	92	--	
		Vo = 4.5 V	--	92	--	

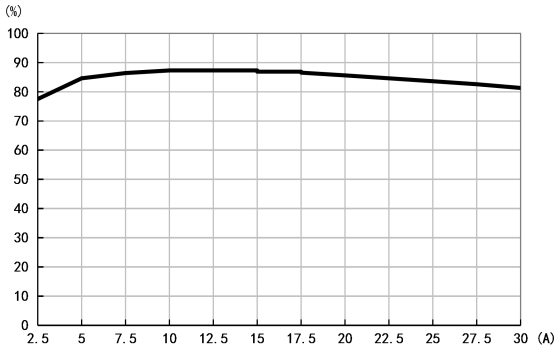
典型特征曲线（双路输出）

V_o = 0.6 V（双路输出）

除非另有说明，以下波形工作条件为：工作温度+25℃，仅使能一路输出，标准配置文件下。

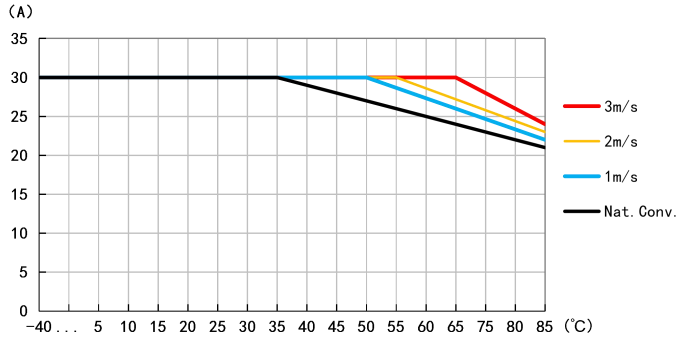
效率

效率 vs. 输出电流，V_{in} = 12 V



温度降额曲线

负载电流 vs. 环境温度和风速，V_{in} = 12 V，另外一路使能满载输 0.6V,

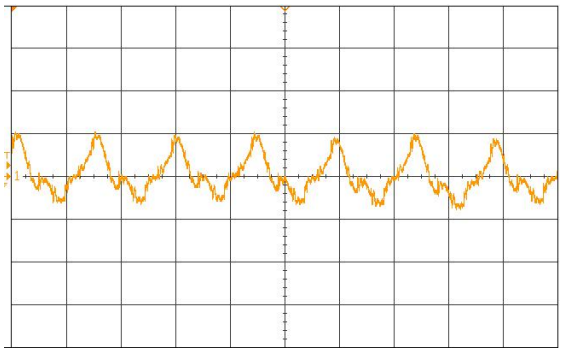


输出纹波和噪声

V_{in} = 12 V, I_o = 30 A,

C_{OUT} = 4 x 330 μF/10 mΩ + 10 x 100 μF

示波器坐标轴：5 mV/div, 2 μs/div, 20 MHz 带宽.

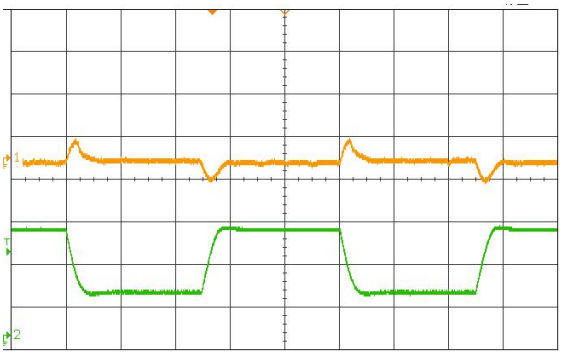


动态响应

输出电压动态响应，负载跳变（25%－75%－25%）

V_{in} = 12 V, C_{OUT} = 4 x 330 μF/10 mΩ + 10 x 100 μF, di/dt = 2 A/μs,

示波器坐标轴：50 mV/div, 10 A/div, 200 μs/div.



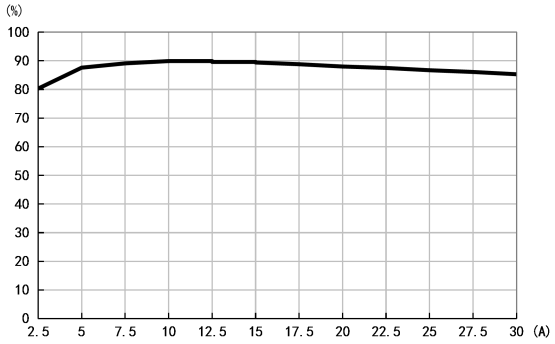
典型特征曲线（双路）

V_o = 1.0 V（双路输出）

除非另有说明，以下波形工作条件为：工作温度+25℃，仅使能一路输出，标准配置文件下。

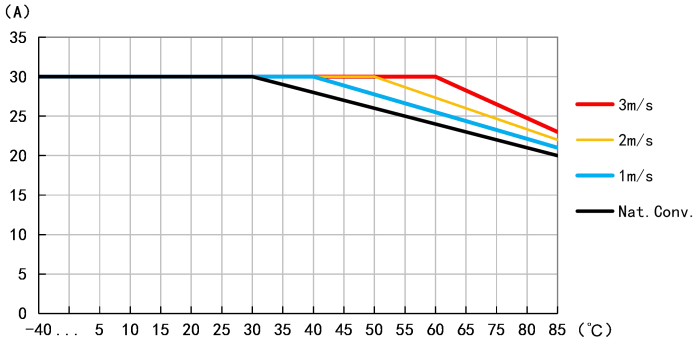
效率

效率 vs. 输出电流，V_{in} = 12 V



温度降额曲线

负载电流 vs. 环境温度和风速，V_{in} = 12 V，另外一路使能满载输出 1.0V，

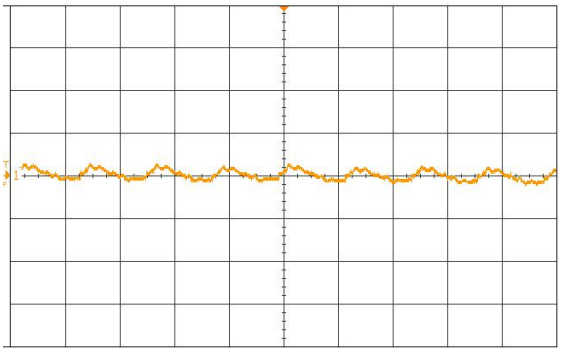


输出纹波和噪声

V_{in} = 12 V, I_o = 30 A,

C_{OUT} = 4 x 330 μF/10 mΩ + 10 x 100 μF

示波器坐标轴：10 mV/div, 2 μs/div, 20 MHz 带宽.

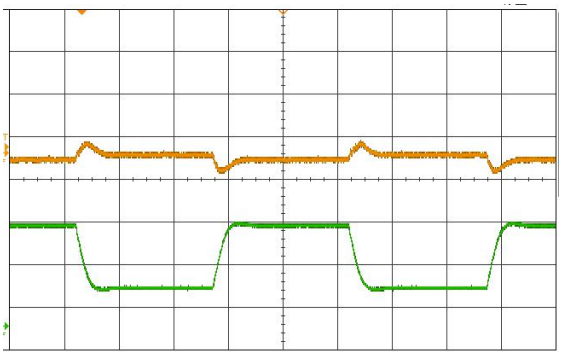


动态响应

输出电压动态响应，负载跳变（25%－75%－25%）

V_{in} = 12 V, C_{OUT} = 4 x 330 μF/10 mΩ + 10 x 100 μF, di/dt = 2 A/μs,

示波器坐标轴：50 mV/div, 10 A/div, 200 μs/div.



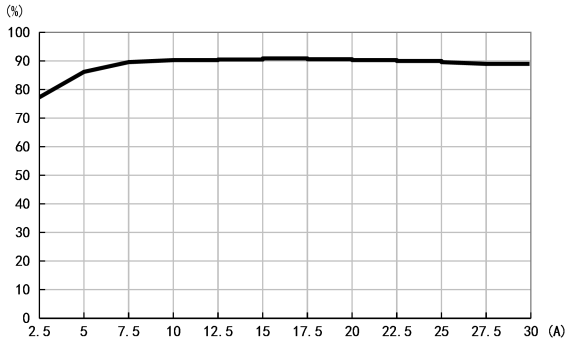
典型特征曲线（双路）

V_o = 1.8 V（双路输出）

除非另有说明，以下波形工作条件为：工作温度+25℃，仅使能一路输出，标准配置文件下。

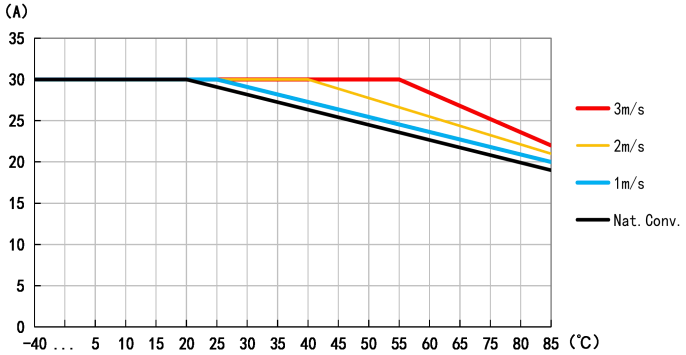
效率

效率 vs. 输出电流，V_{in} = 12 V



温度降额曲线

负载电流 vs. 环境温度和风速，V_{in} = 12 V，另外一路使能满载输出 1.8V，

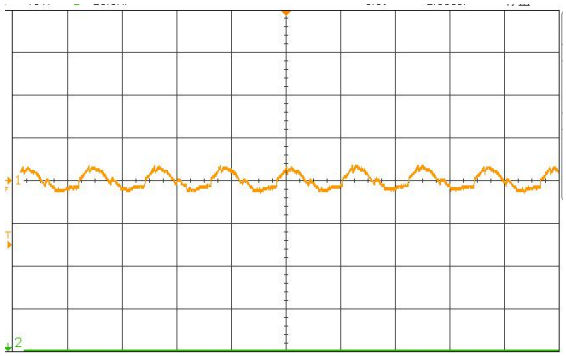


输出纹波和噪声

V_{in} = 12 V, I_o = 30 A,

C_{OUT} = 4 x 330 μF/10 mΩ + 10 x 100 μF

示波器坐标轴：10 mV/div, 2 μs/div, 20 MHz 带宽.

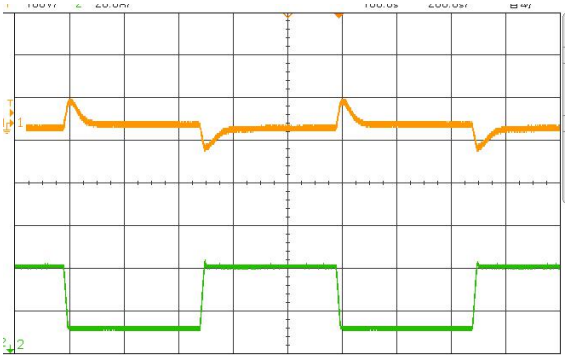


动态响应

输出电压动态响应，负载跳变（25% - 75% - 25%）

V_{in} = 12 V, C_{OUT} = 4 x 330 μF/10 mΩ + 10 x 100 μF, di/dt = 2 A/μs,

示波器坐标轴：50 mV/div, 10 A/div, 200 μs/div.



典型特征曲线（双路）

V_o = 2.5 V（双路输出）

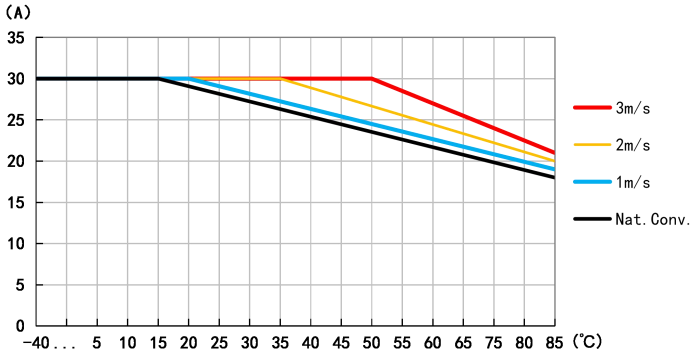
除非另有说明，以下波形工作条件为：工作温度+25℃，仅使能一路输出，标准配置文件下。

效率

效率 vs. 输出电流，V_{in} = 12 V

温度降额曲线

负载电流 vs. 环境温度和风速，V_{in} = 12 V，另外一路使能满载输出 2.5V,

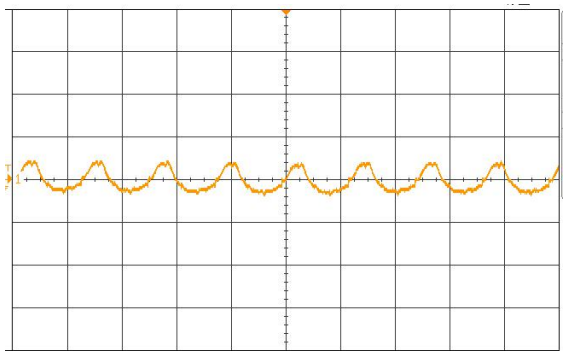


输出纹波和噪声

V_{in} = 12 V, I_o = 30 A,

C_{OUT} = 4 x 330 μF/10 mΩ + 10 x 100 μF

示波器坐标轴：10 mV/div, 2 μs/div, 20 MHz 带宽.

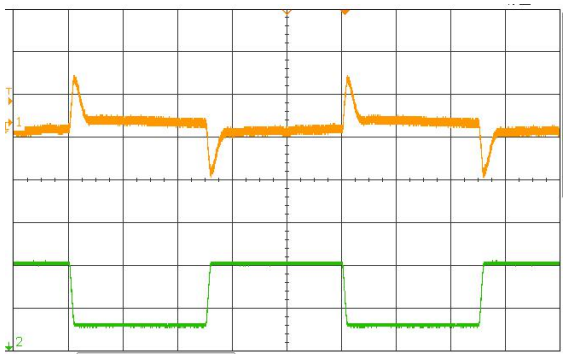


动态响应

输出电压动态响应，负载跳变（25% - 75% - 25%）

V_{in} = 12 V, C_{OUT} = 4 x 330 μF/10 mΩ + 10 x 100 μF, di/dt = 2 A/μs,

示波器坐标轴：50 mV/div, 10 A/div, 200 μs/div.



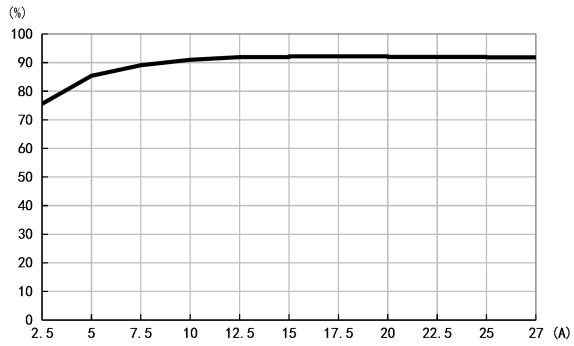
典型特征曲线（双路）

V_o = 3.3 V（双路输出）

除非另有说明，以下波形工作条件为：工作温度+25℃，仅使能一路输出，标准配置文件下。

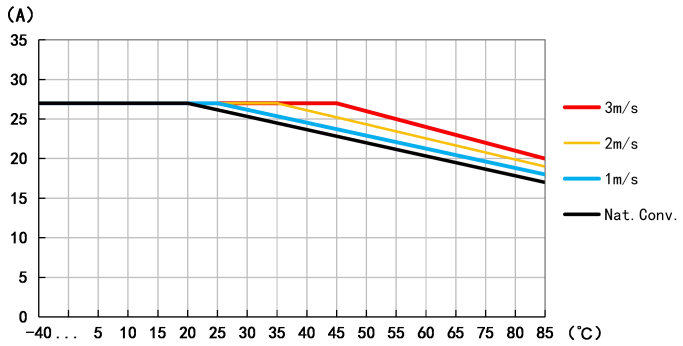
效率

效率 vs. 输出电流，V_{in} = 12 V



温度降额曲线

负载电流 vs. 环境温度和风速，V_{in} = 12 V，另外一路使能满载输出 3.3V，

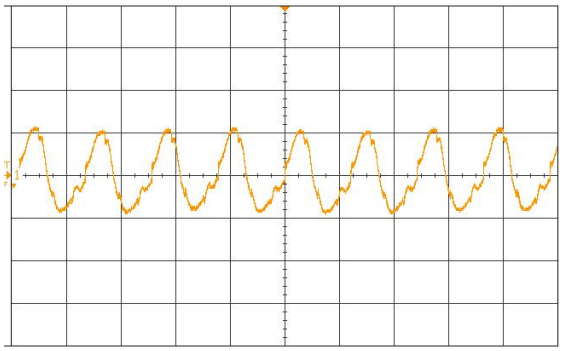


输出纹波和噪声

V_{in} = 12 V, I_o = 27 A,

C_{OUT} = 4 x 330 μF/10 mΩ + 10 x 100 μF

示波器坐标轴：5 mV/div, 2 μs/div, 20 MHz 带宽.

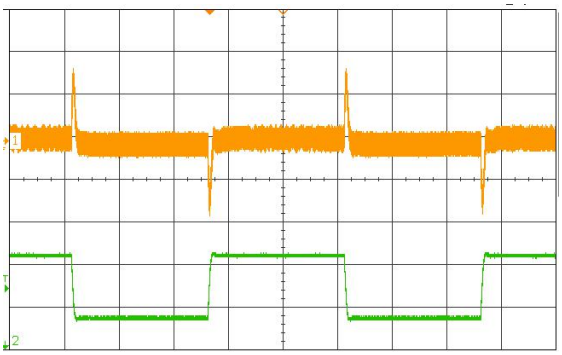


动态响应

输出电压动态响应，负载跳变（25%－75%－25%）

V_{in} = 12 V, C_{OUT} = 4 x 330 μF/10 mΩ + 10 x 100 μF, di/dt = 2 A/μs,

示波器坐标轴：20 mV/div, 10 A/div, 1000 μs/div.



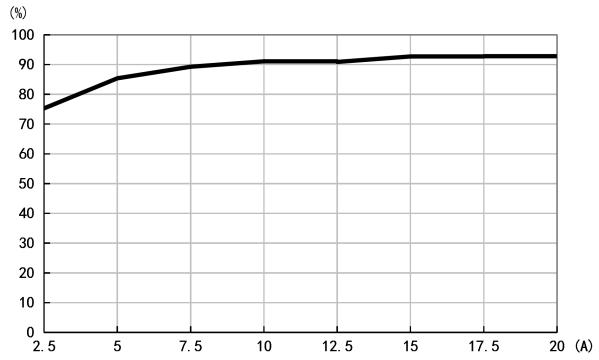
典型特征曲线（双路）

V_o =4.5 V（双路输出）

除非另有说明，以下波形工作条件为：工作温度+25℃，仅使能一路输出，标准配置文件下。

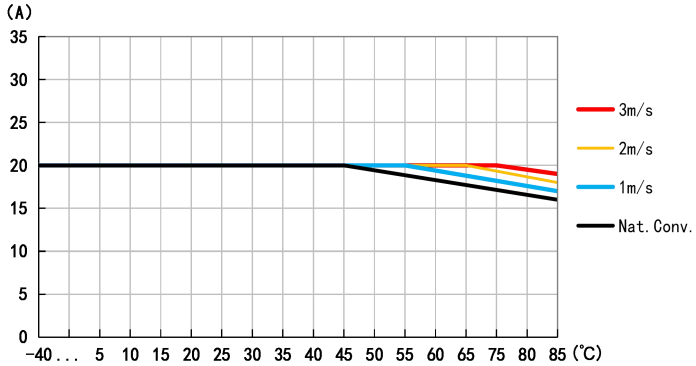
效率

效率 vs. 输出电流，，V_{in} = 12 V



温度降额曲线

负载电流 vs. 环境温度和风速，V_{in}= 12 V，另外一路使能满载输出 4.5V，

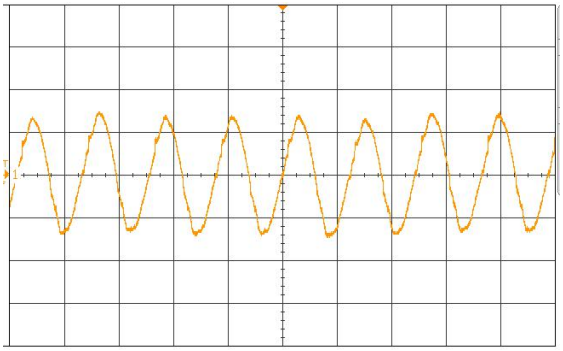


输出纹波和噪声

V_{in} = 12 V, I_o = 20 A,

C_{OUT} = 4 x 330 μF/10 mΩ + 10 x 100 μF

示波器坐标轴：5 mV/div, 2 μs/div, 20 MHz 带宽.

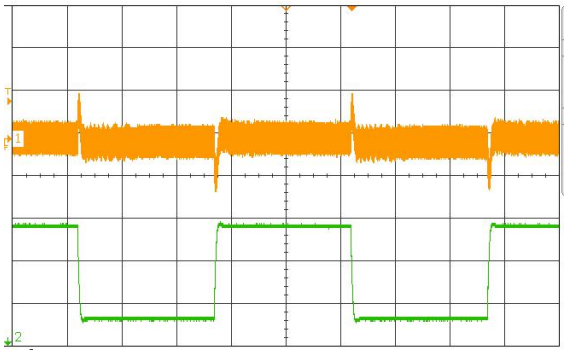


动态响应

输出电压动态响应，负载跳变（25%－75%－25%）

V_{in}= 12 V, C_{OUT}= 4 x 330 μF/10 mΩ + 10 x 100 μF, di/dt = 2 A/μs,

示波器坐标轴：20 mV/div, 5 A/div, 1000 μs/div.



典型开关机波形（双路输出）

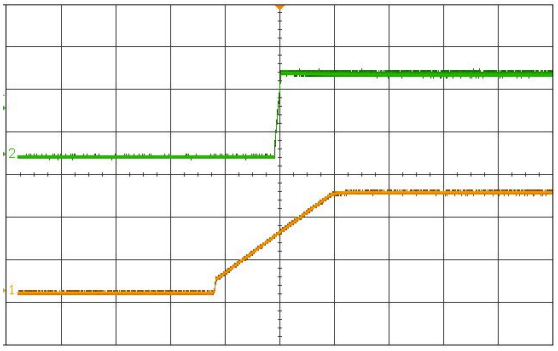
V_o = 1.0 V（双路输出）

除非另有说明，以下波形工作条件为：工作温度+25℃，仅使能一路输出，标准配置文件下。

开机波形

V_{in} = 12 V, I_o = 30 A.

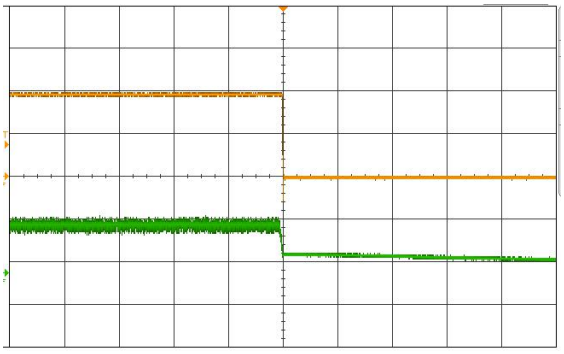
示波器坐标轴：0.5V/div（Vo），5 V/div（Vin），20 ms/div.



关机波形

V_{in} = 12 V, I_o = 30 A

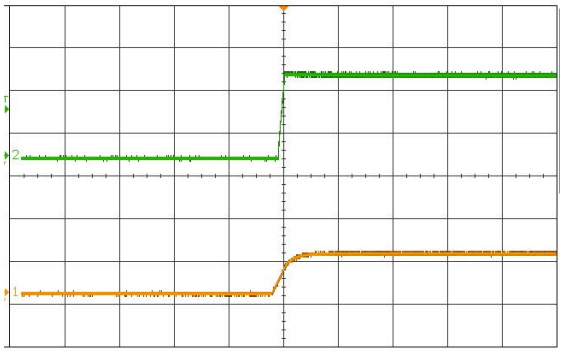
示波器坐标轴：0.5V/div（Vo），10 V/div（Vin），20 ms/div.



CNTL 开启波形

V_{in} = 12 V, I_o = 30 A.

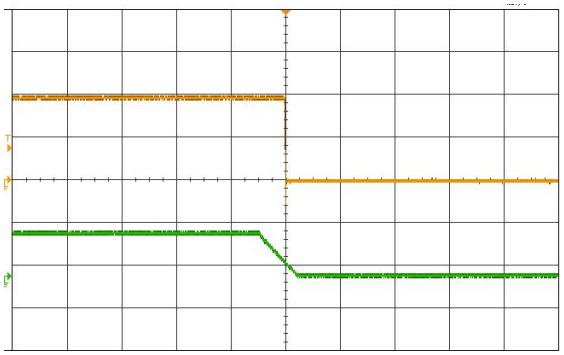
示波器坐标轴：0.5V/div（Vo），5 V/div（CNTL），20 ms/div.



CNTL 关断波形

V_{in} = 12 V, I_o = 30 A.

示波器坐标轴：0.5V/div（Vo），5 V/div（CNTL），20 ms/div.



产品电气特性（单路输出）

以下部分规格与产品的数字控制相关，可用于可配置参数的 PMBus 命令已用大写字母标注。

若无特殊说明，以下规格的工作温度范围为-40 至+85℃，输入电压为 7.5 至 14.4 V，频率为 430KHz；以下规格的典型值的工作条件为工作温度 +25℃，输入电压 12.0 V，满载输出；另外输出电压需在引脚上测量，数字控制为标准配置文件，仅使能一路输出。

另外需求外接 C_{IN} = 2x470 uF/10 mΩ OS-CON + 10 x 10 uF 陶瓷电容，C_{OUT} =8 x 330 uF/10 mΩ Polymer + 20 x 100 uF 陶瓷电容，如典型应用电路图。

规格		条件	最小值	典型值	最大值	单位
输入电压						
V_{in}	输入电压		7.5	12	14.4	V
	输入电压上升时间	单调上升	--	--	10	V/ms
输出电压						
V_o	输出电压可调范围	分压电阻配置	0.6	--	4.5	V
		分压电阻 / PMBus 配置	0.54	--	4.5	V
	输出电压设置精度		--	±0.025	--	%V_o
	输出电压精度/偏差	1.0V≤Vo≤4.5V	-1	--	+1	%V_o
		Vo<1.0V	-10	--	10	mV
	线性调整率	Vo = 0.6 V	--	1	--	mV
		Vo = 1.0 V	--	2	--	
		Vo = 1.8 V	--	2	--	
		Vo = 2.5 V	--	3	--	
		Vo = 3.3 V	--	3	--	
		Vo = 4.5 V	--	3	--	
	负载调整率	Vo = 0.6 V	--	1	--	
		Vo = 1.0 V	--	1	--	
		Vo = 1.8 V	--	1	--	
		Vo = 2.5 V	--	2	--	
		Vo = 3.3 V	--	3	--	
		Vo = 4.5 V	--	3	--	
V_{o-ac}	输出纹波&噪声（20MHz 带宽下）	Vo = 0.6 V	--	7	--	mVp-p
		Vo = 1.0 V	--	8	--	
		Vo = 1.8 V	--	12	--	
		Vo = 2.5 V	--	14	--	
		Vo = 3.3 V	--	16	--	
		Vo = 4.5 V	--	19	--	
温度漂移系数		工作温度范围-40℃ to +85℃	--	±0.2	--	%/℃
瞬态响应偏差		标称输入电压，25%负载跳变	--	30	--	mV
瞬态恢复时间			--	1	--	us
输入电流						
$I_{in-no\ load}$	输入空载电流	Vo = 0.6 Vdc	--	160	--	mA
		Vo = 4.5 Vdc	--	300	--	mA
I^2t	瞬时冲击电流		--	--	1	A^2s
输出电流						
I_o	输出电流（每路）	Vo = 0.6 V	0	--	60	A
		Vo = 1.0 V	0	--	60	A

		Vo = 1.8 V	0	--	60	A
		Vo = 2.5 V	0	--	60	A
		Vo = 3.3 V	0	--	54	A
		Vo = 4.5 V	0	--	40	A
I_{lim}	输出电流限制阈值（每路）	OCP 阈值设置为 50 A	--	100	--	A
效率						
η	效率 max I_o	Vo = 0.6 V	--	82	--	%
		Vo = 1.0 V	--	86	--	
		Vo = 1.8 V	--	90	--	
		Vo = 2.5 V	--	91	--	
		Vo = 3.3 V	--	92	--	
		Vo = 4.5 V	--	92	--	

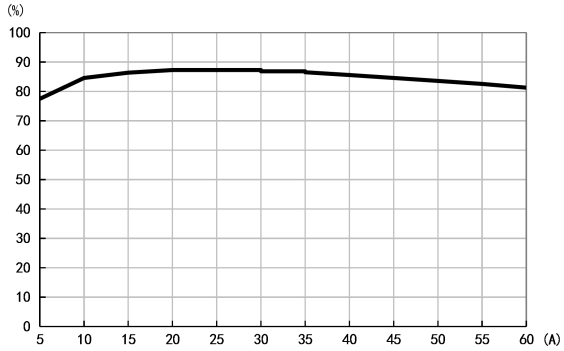
典型特征曲线（单路输出）

V_o = 0.6 V（单路输出）

除非另有说明，以下波形工作条件为：工作温度+25℃，标准配置文件下。

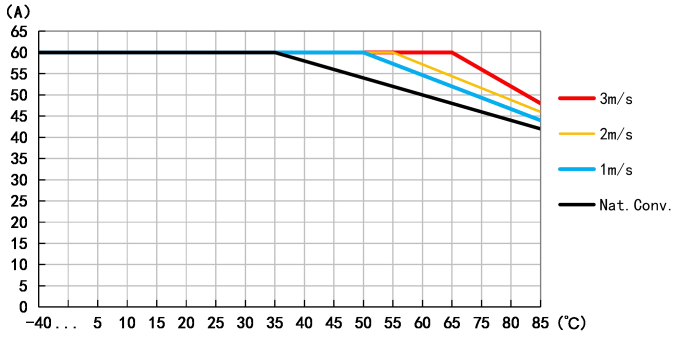
效率

效率 vs. 输出电流，V_{in} = 12 V



温度降额曲线

负载电流 vs. 环境温度和风速，V_{in} = 12 V

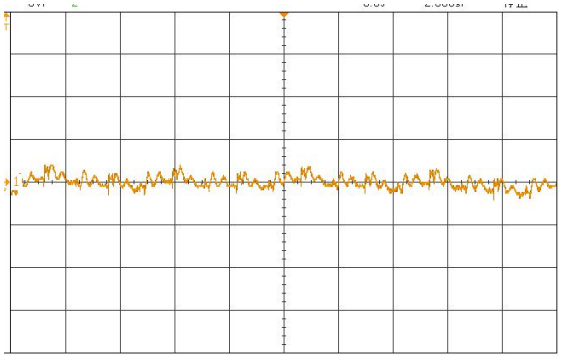


输出纹波和噪声

V_{in} = 12 V, I_o = 60 A,

C_{OUT} = 8 x 330 μF/10 mΩ + 20 x 100 μF

示波器坐标轴：5 mV/div, 2 μs/div, 20 MHz 带宽.

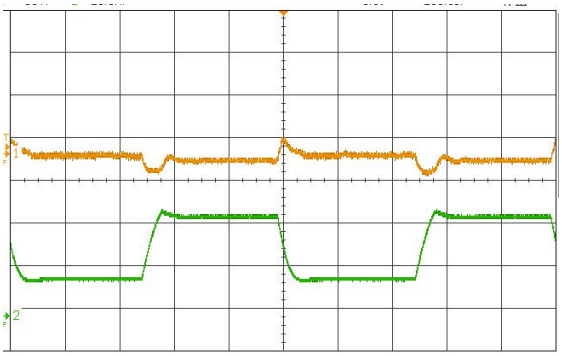


动态响应

输出电压动态响应，负载跳变（25% - 75% - 25%）

V_{in} = 12 V, C_{OUT} = 8 x 330 μF/10 mΩ + 20 x 100 μF, di/dt = 2 A/μs,

示波器坐标轴：50 mV/div, 20 A/div, 200 μs/div.



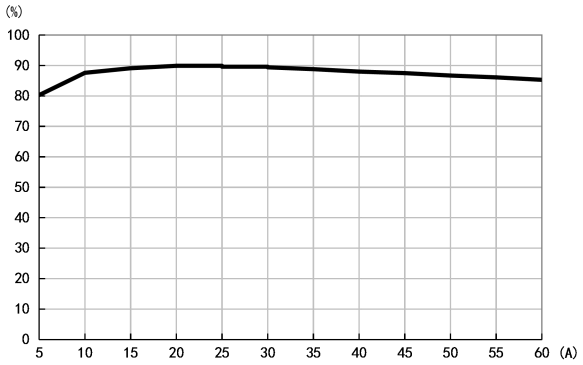
典型特征曲线（单路）

V_o = 1.0 V（单路输出）

除非另有说明，以下波形工作条件为：工作温度+25℃，标准配置文件下。

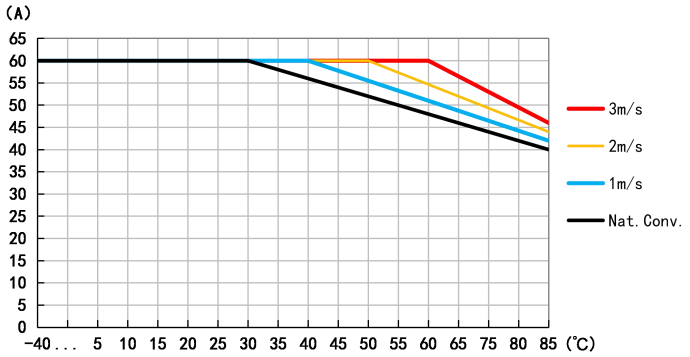
效率

效率 vs. 输出电流，V_{in} = 12V



温度降额曲线

负载电流 vs. 环境温度和风速，V_{in} = 12 V

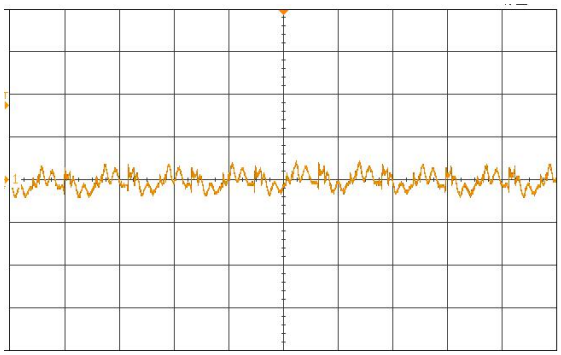


输出纹波和噪声

V_{in} = 12 V, I_o = 60 A,

C_{OUT} = 8 x 330 μF/10 mΩ + 20 x 100 μF

示波器坐标轴：5 mV/div, 2 μs/div, 20 MHz 带宽.

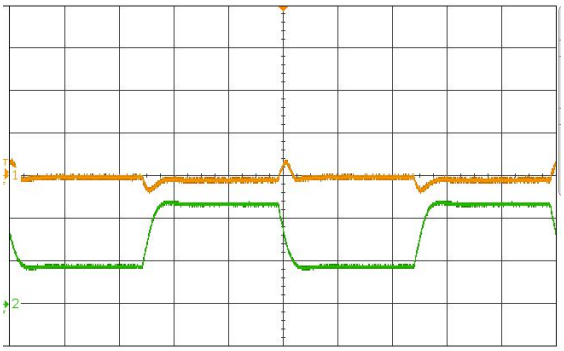


动态响应

输出电压动态响应，负载跳变（25% - 75% - 25%）

V_{in} = 12 V, C_{OUT} = 8 x 330 μF/10 mΩ + 20 x 100 μF, di/dt = 2 A/μs,

示波器坐标轴：50 mV/div, 20 A/div, 200 μs/div.



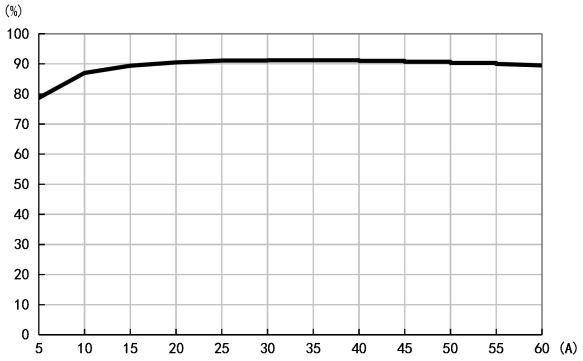
典型特征曲线（单路）

V_o = 1.8 V（单路输出）

除非另有说明，以下波形工作条件为：工作温度+25℃，标准配置文件下。

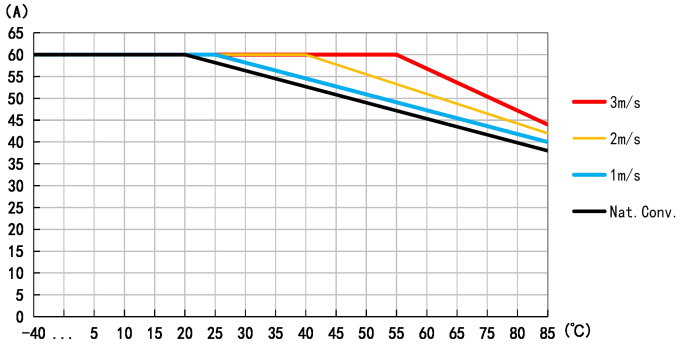
效率

效率 vs. 输出电流，V_{in} = 12 V



温度降额曲线

负载电流 vs. 环境温度和风速，V_{in} = 12 V

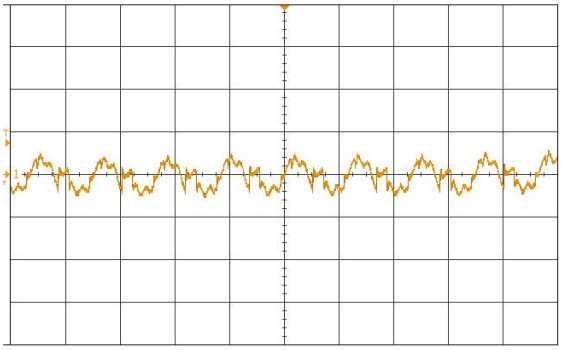


输出纹波和噪声

V_{in} = 12 V, I_o = 60 A,

C_{OUT} = 8 x 330 μF/10 mΩ + 20 x 100 μF

示波器坐标轴：5 mV/div, 2 μs/div, 20 MHz 带宽.

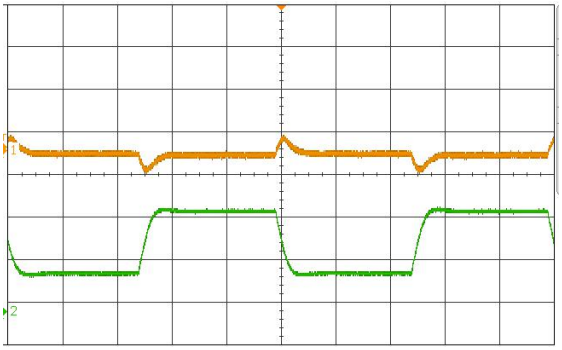


动态响应

输出电压动态响应，负载跳变（25% - 75% - 25%）

V_{in} = 12 V, C_{OUT} = 8 x 330 μF/10 mΩ + 20 x 100 μF, di/dt = 2 A/μs,

示波器坐标轴：50 mV/div, 20 A/div, 200 μs/div.



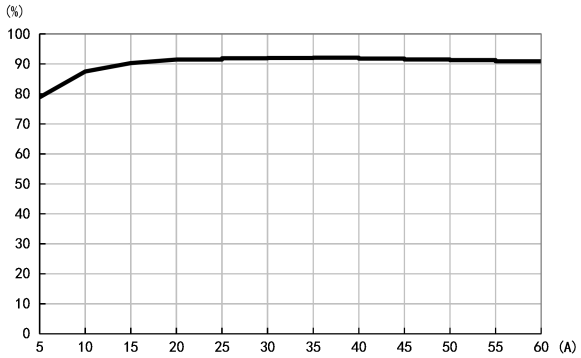
典型特征曲线（单路）

V_o = 2.5 V（单路输出）

除非另有说明，以下波形工作条件为：工作温度+25℃，标准配置文件下。

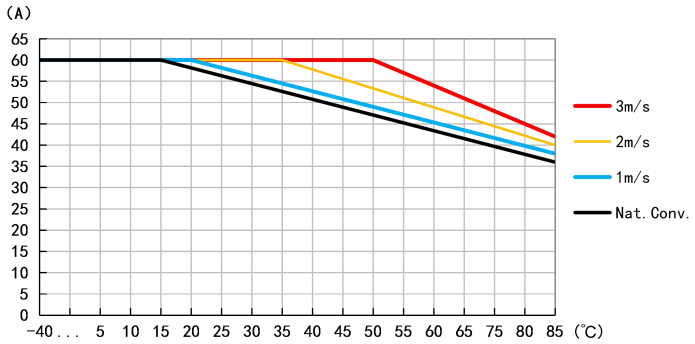
效率

效率 vs. 输出电流，V_{in} = 12 V



温度降额曲线

负载电流 vs. 环境温度和风速，V_{in} = 12 V

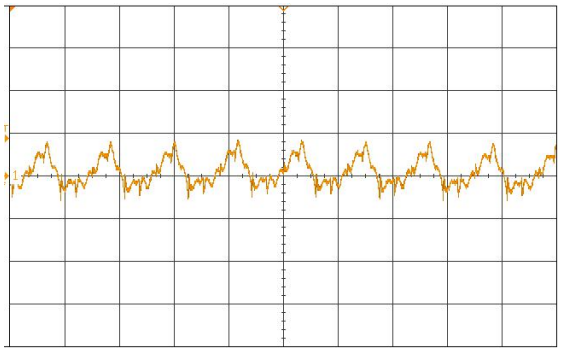


输出纹波和噪声

V_{in} = 12 V, I_o = 60 A,

C_{OUT} = 8 x 330 μF/10 mΩ + 20 x 100 μF

示波器坐标轴：5 mV/div, 2 μs/div, 20 MHz 带宽.

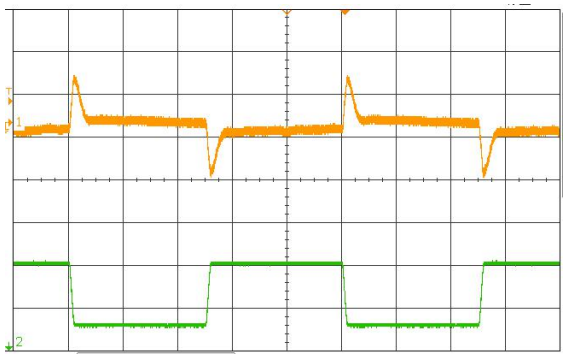


动态响应

输出电压动态响应，负载跳变（25% - 75% - 25%）

V_{in} = 12 V, C_{OUT} = 8 x 330 μF/10 mΩ + 20 x 100 μF, di/dt = 2 A/μs,

示波器坐标轴：50 mV/div, 20 A/div, 200 μs/div.



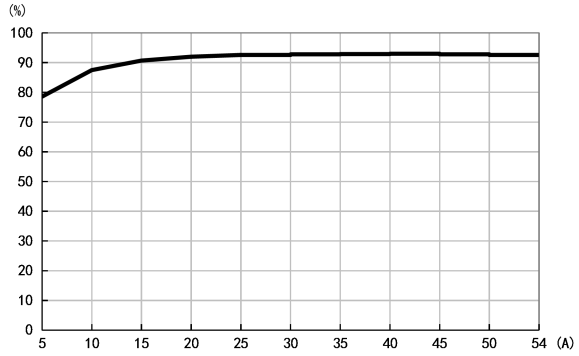
典型特征曲线（单路）

V_o = 3.3 V（单路输出）

除非另有说明，以下波形工作条件为：工作温度+25℃，标准配置文件下。

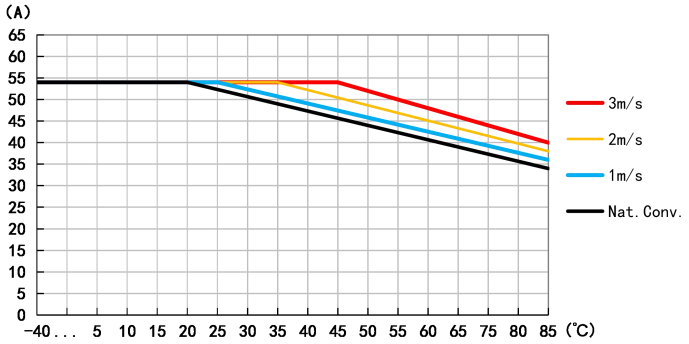
效率

效率 vs. 输出电流，V_{in} = 12 V



温度降额曲线

负载电流 vs. 环境温度和风速，V_{in} = 12 V

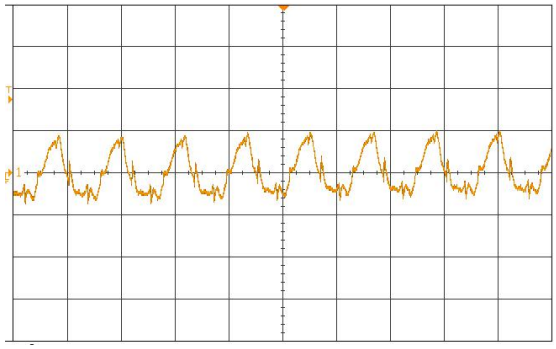


输出纹波和噪声

V_{in} = 12 V, I_o = 54 A,

C_{OUT} = 8 x 330 μF/10 mΩ + 20 x 100 μF

示波器坐标轴：5mV/div, 2 μs/div, 20 MHz 带宽.

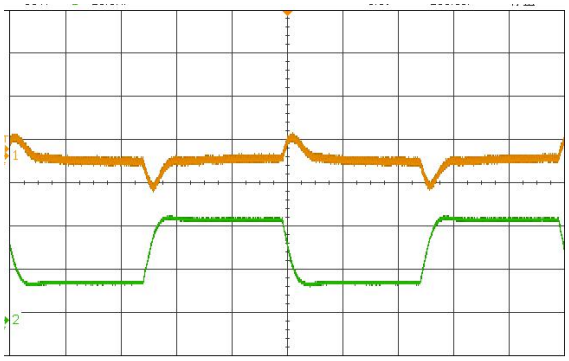


动态响应

输出电压动态响应，负载跳变（25% - 75% - 25%）

V_{in} = 12 V, C_{OUT} = 8 x 330 μF/10 mΩ + 20 x 100 μF, di/dt = 2 A/μs,

示波器坐标轴：50 mV/div, 20 A/div, 200 μs/div.



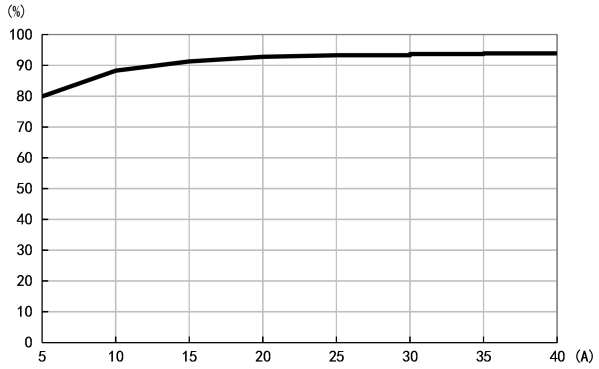
典型特征曲线（单路）

V_o = 4.5 V（单路输出）

除非另有说明，以下波形工作条件为：工作温度+25℃，标准配置文件下。

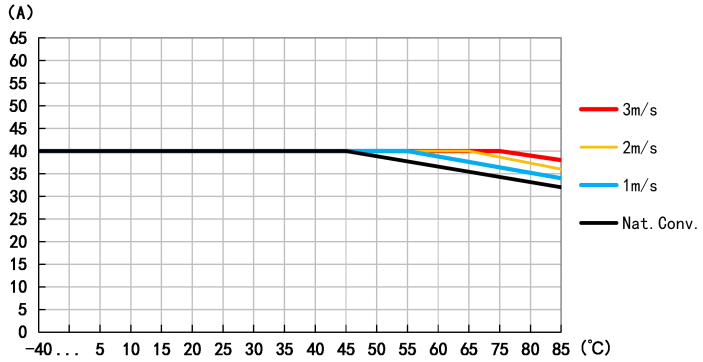
效率

效率 vs. 输出电流，V_{in} = 12 V



温度降额曲线

负载电流 vs. 环境温度和风速，V_{in} = 12 V

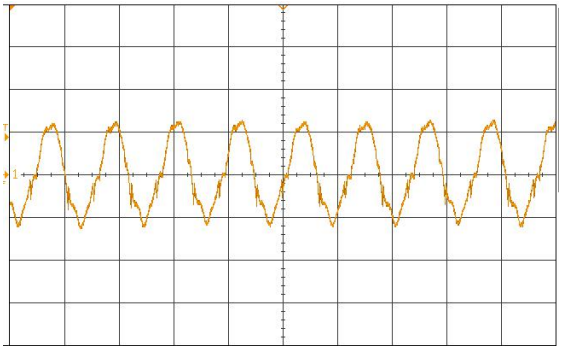


输出纹波和噪声

V_{in} = 12 V, I_o = 40 A,

C_{OUT} = 8 x 330 μF/10 mΩ + 20 x 100 μF

示波器坐标轴：5 mV/div, 2 μs/div, 20 MHz 带宽.

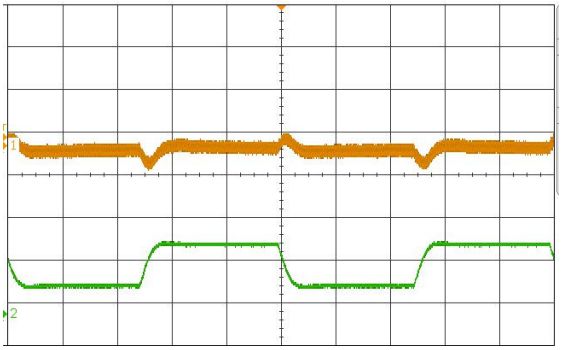


动态响应

输出电压动态响应，负载跳变（25% - 75% - 25%）

V_{in} = 12 V, C_{OUT} = 8 x 330 μF/10 mΩ + 20 x 100 μF, di/dt = 2 A/μs,

示波器坐标轴：50 mV/div, 20 A/div, 200 μs/div.



典型开关机波形（单路输出）

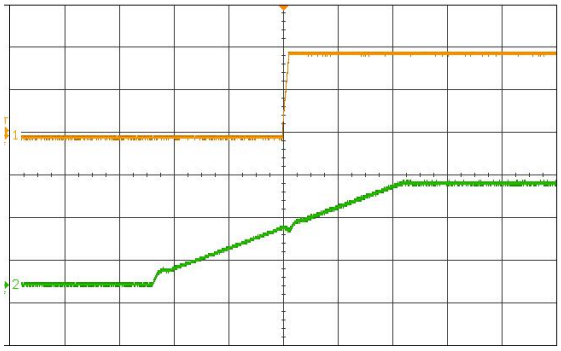
V_o = 1.0 V（单路输出）

除非另有说明，以下波形工作条件为：工作温度+25℃，标准配置文件下。

开机波形

V_{in} = 12 V, I_o = 60 A.

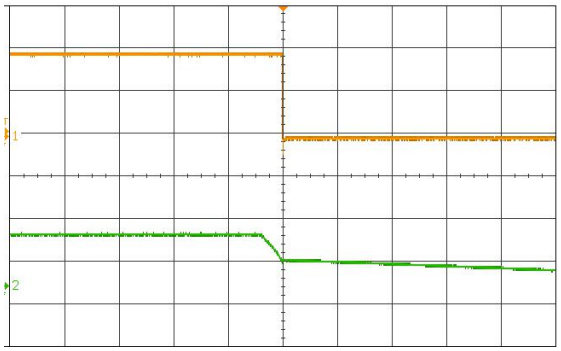
示波器坐标轴：0.5V/div（Vo），5 V/div（Vin），20 ms/div.



关机波形

V_{in} = 12 V, I_o = 60 A.

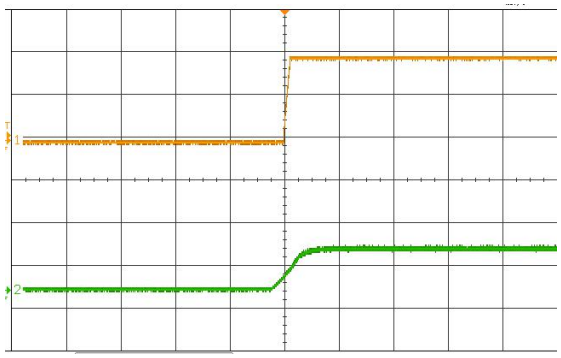
示波器坐标轴： 0.5V/div（Vo），10 V/div（Vin），20 ms/div.



CNTL 开启波形

V_{in} = 12 V, I_o = 60 A.

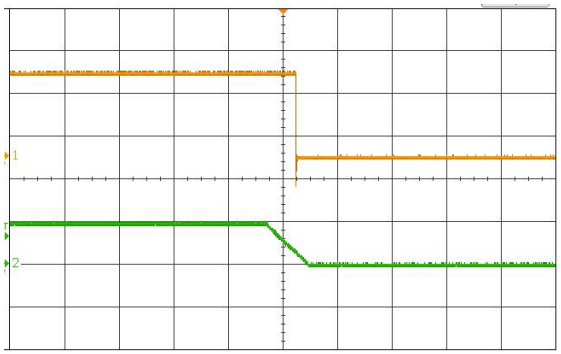
示波器坐标轴：0.5V/div（Vo），5 V/div（CNTL），20 ms/div.



CNTL 关断波形

V_{in} = 12 V, I_o = 60 A.

示波器坐标轴： 0.5V/div（Vo），5 V/div（CNTL），20 ms/div.



PMBus 接口

PMBus 基本特性

PMBus 的时序和电气特性可以在 PMBus 电源管理协议规范，第 1 部分，修订 1.1 中找到，请访问 http://PMBus.org 查看。模块可同时支持 100 kHz 和 400 kHz 的总线速度要求，且模块在与主板通信时不拉伸 PMBus 上的脉冲。

通过 KD12T-60A 模块的 PMBus 接口进行通信时可以支持包错误检查（PEC）。如果主板为 PEC 字节提供 CLK 脉冲，则使用 PEC。如果 CLK 脉冲在 STOP 之前不存在，则不使用 PEC。

KD12T-60A 模块支持 PMBus 1.1 规范中的命令子集。大多数参数可以使用 PMBus 进行配置，并存储为默认值供以后使用。所有需要数据输入或输出的命令都使用文字格式。数据字的指数固定在命令的合理值，不支持更改指数。KD12T-60A 模块不支持直接格式数据输入或输出。有关详细信息，请参阅支持的 PMBus 命令部分。

KD12T-60A 模块还支持 SMBALERT 响应协议。通过该协议机制，KD12T-60A 模块可以与总线主板模块进行通信。主板模块处理此事件，并通过警报响应地址同时访问总线上（支持该协议）的所有从模块。只有引起警报的从服务器承认此请求。主机执行修改后的接收字节操作来获取从服务器的地址。此时，主服务器可以使用 PMBus 状态命令来查询引起警报的从服务器。有关 SMBus 警报响应协议的更多信息，请参阅系统管理总线（SMBus）规范。

KD12T-60A 模块包含非易失性存储器，用于存储配置文件。不过，写入模块的设置不会自动保存到这个非易失性存储器中。必须使用 STORE_USER_ALL 命令将当前配置作为模块默认值提交到非易失性内存，能够存储在非易失性存储器中的设置在其详细描述中加以说明。

PMBus 地址位

PMBus 规范要求在 PMBus 总线上的每个模块都有一个唯一的地址 ID。KD12T-60A 模块有 64 个可配置的地址（十进制为 0 到 63），可以通过将 ADDR0 和 ADDR1 引脚的电阻连接到 AGND 来分配。地址以两个八进制（0-7）数字的形式设置，每个引脚一个数字。ADDR1 是高阶数字，ADDR0 是低阶数字。

在 PMBus 通信时，KD12T-60A 模块的 PMBus 地址为'0b'+ADDR1+ADDR0。PMBus 协议的 R/W 位被添加在地址的末尾，使其净 8 位宽。

电阻与数字位关系如下表所示：：

数字	电阻（kΩ）
0	8.45
1	16.2
2	25.5
3	37.4
4	54.9
5	84.5
6	133
7	200

KD12T-60A 还可以检测出 ADDR0 和 ADDR1 引脚上超出范围的值，如果任何一个地址引脚被检测到超出范围的电阻值连接至它，模块将会继续响应 PMBus 指令，但地址位会被设置在 127，这可能会在配置地址之外，这种情况下的模块是可以运行的，但不建议，特别是如果总线上还有其他的模块占用了 127 这个地址位。

注意：一些地址被 SMBus 规范保留，不能被模块使用或分配，有关更多信息，请参阅 SMBus 规范。

PMBus 连接

KD12T-60A 模块同时支持 100 kHz 和 400 kHz 总线速度。PMBus 接口的连接遵循系统管理总线（SMBus）规范 V2.0 中给出的 400 kHz 总线速度的高功率直流规范或 3.1.2 节中的 100kHz 总线速度的低功率直流规范。完整的 SMBus 规范可从 SMBus 网站 smbus.org 获得。

PMBus 数据格式

PMBus 表单命令支持三种数据格式，它们需要以文字数字表示作为参数（设置阈值、电压或报告此类命令）。兼容模块只需要支持其中一种格式即可。KD12T-60A 模块仅支持这些命令的线性数据格式。在这种格式中，data 参数由尾数和指数两部分组成。该参数表示的数字可以表示为:

$$Value = Mantissa \times 2^{exponent}$$

操作指南

输入欠压保护 （UVLO）

输入 UVLO 开启/关断阈值通过 PMBus VIN_ON 和 VIN_OFF 命令设置。在三相和四相应用中，这些命令必须设置为一致。

外置输入电容

BUCK 变换器的输入纹波 RMS 电流可以估算为：

$$I_{inputRMS} = I_{load}\sqrt{D(1-D)} \quad (\text{valid for } D<1, \text{single-phase})$$

$$I_{inputRMS} = I_{load}\sqrt{D(0.5-D)} \quad (\text{valid for } D<0.5, \text{two-phase})$$

其中，I_{load}为输出负载电流，D 为占空比。

对于大多数应用，非坦电容是首选的，因为这种电容的稳定性可以适应由极低阻抗源供电系统的产生的高涌流。推荐使用陶瓷电容和低 ESR 的电解/聚合物电容并联。陶瓷电容的低 ESR 可有效地限制输入电压纹波，而电解电容最大限度地减少了大负载瞬态变化时输入电压的变化。

在多相应用下，每个产品的输入纹波电流和输入电容值可以降低，如上公式所示。

另外输入的陶瓷电容必须放置紧密，并与 VIN 和 GND 引脚低阻抗连接，以便有效降低输入纹波。

外置输出电容

输出电容的要求取决于两个因素：输出电压纹波和负载瞬态响应。为了实现较低的输出电压纹波，输出电容必须使用低 ESR 的电容，而且低 ESR 的电容还可实现更小的负载瞬态响应变化。若对负载瞬态变化的要求不高时，可以减少外围的输出电容，而对负载瞬态变化的要求比较高时，可以使用更多的输出电容来实现更小的瞬态变化。另外还可以通过调整产品的控制环路来改善瞬态响应偏差，增加输出电容降低环路带宽。

建议将低 ESR 的陶瓷电容和低 ESR 的电解/聚合物电容放置在尽可能靠近产品输出端&远端补偿的位置，并并联多个电容以降低其 ESR。为了使电容更有效，需要使用低阻抗和低感抗的 PCB 布局和布线。

远端补偿

该产品具有远端补偿功能，可补偿由于产品输出端和负载之间的寄生阻抗导致的输出电压下降。VSNS 和 GSNS 应布置为差分对，最好有 PCB 接地层进行屏蔽，以降低噪声敏感性。

开关机

模块的启动和关断可由操作命令、CNTL 引脚或输入电压共同控制。另外还可以通过 PMBus 命令配置开机延迟和关机延迟。

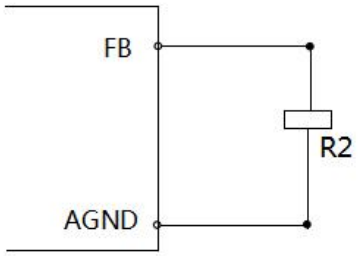
注意：

如果模块由于关机延迟时间而未完全关断，应避免在关机延迟时间到期之前尝试打开模块。只有在关机延迟时间到期且模块已经关闭后，模块才

可以被再次打开。对于三相和四相配置下，两个模块的开关延迟时间必须配置为相同的值。

输出电压调节

FB 引脚连接到内部误差放大器的输入端，内部参考电压为 600 mV±0.5%。



$$R2 = R_{FBX}(k\Omega) = \frac{6}{V_O - V_{FB}}$$

模块的输出电压可以使用 VREF_TRIM 命令进行调节，该命令的格式详见 MFR_SPECIFIC_04 （VREF_TRIM） （D4h）说明，其调节范围在输出电压的-20%到 10%之间， VREF_TRIM 命令通常用于精调模块的输出电压，步进为 2mV。另外 MARGINING 和 VREF_TRIM 共同限制了输出电压可调范围在-30%到 10%之间，不建议超过该范围。

KD12T-60A 可以通过以下三种形式确定实际的输出电压：

- **No output margin**

$$V_{FB} = VREF\_TRIM + 0.6$$

- **Margin High Voltage State**

$$V_{FB} = STEP\_VREF\_MARGIN\_HIGH + VREF\_TRIM + 0.6$$

- **Margin Low State**

$$V_{FB} = STEP\_VREF\_MARGIN\_LOW + VREF\_TRIM + 0.6$$

- VFB 是 FB 引脚上的电压
- VREF_TRIM 是输出电压的偏置电压
- VREF_MARGIN_HIGH 是输出电压可调的边际电压上限
- VREF_MARGIN_LOW 是输出电压可调的边际电压下限

输出过压/欠压保护

KD12T-60A 通过测量 FB 引脚上的电压，以提供输出欠压和输出过压保护。欠压阈值与参考电压成正比例，过压阈值可以设置为固定值，也可以设置为与参考电压成正比例的值。

输出欠压保护方案与输出过流保护方案相同。当欠压故障被触发时，高侧和低侧 MOS 都被关闭。IOUT_OC_FAULT_RESPONSE 的配置决定模块对 UV 故障的响应。如果 IOUT_OC_FAULT_RESPONSE 被设置为在 OC 故障后重新启动模块，那么模块也被配置为在 UV 故障后重新启动，另外只有在软启动完成

后才可触发 UV 保护。

当 OV 故障触发时，高侧 MOS 关闭，低侧 MOS 保持打开以对输出放电。模块保持低侧 MOS 导通，直到输入电源切换或 CNTL 引脚切换或 PMBus 命令切换。这种机制保护了输出免受过电压的影响。当 OV 阈值为固定值时，OV 保护随时处于激活状态。当 OV 阈值与参考电压成比例时，只有在软启动后才启用 OV 保护。在多相模式下，仅检测主机的 FB 引脚的输出电压的 UV 和 OV 故障。任何从机均无法检测输出电压相关的故障。有关更多信息，请参阅 MFR_SPECIFIC_07 （PCT_VOUT_FAULT_PG_LIMIT） （D7h）和（E0h） MFR_SPECIFIC_16 （COMM_EEPROM_SPARE）部分。

PGOOD 指示

KD12T-60A 通过测量 FB 引脚上的电压来指示输出电压是否处于正常状态。在软启动过程中，PG 引脚被拉到 GND。在标准配置文件下，若软启动时间完成后，如果输出电压在 PGOOD 窗口内（PG_Low 和 PG_High 之间），PG 引脚在 2ms 延迟时间后释放。可以使用 MFR_SPECIFIC_16 寄存器禁用 2 毫秒的延迟。当输出电压低于 PG_Low 或高于 PG_High 时，PG 引脚立即被拉到地。PG_Low 和 PG_High 值可以通过 PMBus 命令 MFR_SPECIFIC_07 （PCT_VOUT_FAULT_PG_LIMIT）设置。

过流保护

过电流保护采用两种保护方式。当峰值电流超过设定的阈值时，实现逐周期限流。PMBus 使用 IOUT_OC_FAULT_LIMIT 和 IOUT_OC_WARN_LIMIT 命令设置当前限制阈值。在 7 次 OC 计数后，模块关闭高侧和低侧 MOS，并默认进入打嗝模式。如果在软启动操作期间检测到 OC，则仅进入逐周期电流限制。

IOUT_OC_FAULT_RESPONSE PMBus 命令可对 OC 故障的响应进行配置。模块可以被配置为锁存直到输入电源或 CNTL 切换,或者关闭并尝试在延迟 7 × tON_RISE 后重新启动。当通道 2 被配置为从机时，该寄存器不能被配置。在通道 2 为从机的情况下，通道 1 的故障响应设置将自动应用到通道 2。对于三相和四相配置，两个模块都必须配置成一致的命令才可以进行正确的故障响应。

时钟同步和相位设置

开关频率可以通过 SYNC 引脚上的外部时钟同步。在单相、两相或四相工作时，SYNC 信号的频率必须是开关频率的 4 倍，在三相工作时必须是开关频率的 3 倍。SYNC 信号必须是占空比为 50%的方形波形。高电平阈值应大于 2V，低电平阈值应小于 0.8 V。SYNC 和 PHSET 设置的更改仅在电源重启后生效。

在三相和四相应用中，模块通过将主机的 SYNC 引脚和 PHSET 引脚连接到从机上相应的引脚来实现两个模块之间的时钟和相位同步。相位配置由 PMBus 命令 MFR_SPECIFIC_22 （E6h）设置。

软启动时间

KD12T-60A 模块可配置软启动时间，由 TON_RISE PMBus 命令从 600 us 到 9 ms 可选配置，详细信息可参阅命令说明。在选择软启动时间时，应考虑输出电容上的充电电流，在有大量输出电容的应用下，这种电流会导致过流保护而关断模块。故为确保这些问题不会发生，在考虑过流阈值设置时，应考虑输出电容的充电电流。输出电容的充电电流由下式可得:

$$I_{CAP} = \frac{V_{OUT} \times C_{OUT}}{t_{SS}}$$

•ICAP 为输出电容的充电电流，单位为 A

•VOUT 为模块的输出电压，单位为 V

•COUT 为输出电容的总容值，单位为 F

•tSS 为所选的软启动时间，单位为 s

计算出充电电流后，可将过流阈值配置为最大负载电流和输出电容充电电流之和并留一定余量。所需保证的余量可取决于特定的应用场合，但建议为 25%。

注意：对于三相和四相配置时，两个模块的软启动时间必须配置为相同的值。

开关机延迟和电源排序

KD12T-60A 模块提供了许多电源排序的方案。可使用 ON_OFF_CONFIG 命令，或 CNTL 引脚上的信号，或通过 PMBus 的 OPERATION 命令。

当输入电压达到 ON_OFF_CONFIG 所配置的开启阈值，开启延迟可以通过 TON_DELAY 设置。上升时间可以用 TON_RISE 配置。当输入电压达到所配置的关断阈值时，可以使用 TOFF_DELAY 配置关断延迟。更多信息可以在 PMBus 命令描述中找到。

当启动后输出电压在 PGOOD 限制范围内时，PGOOD 引脚被开路。这可以在双路输出模式下连接到另一个通道的 CNTL 引脚以控制开断顺序。

电流共享

多相应用下，所有通道共享相同的误差放大器输出电压（VCOMP）。每个通道的电流首先在电流共享电路中进行比较，然后与误差放大器进行比较并输入 COMP，得到的误差电压与电压斜坡进行比较以以生成 PWM 脉冲。

故障通信

当 OC、VIN_UV、VOUT_UV 或 OT 故障时，对应通道的 FLT 引脚内部拉低。此外如果任何通道的 FLT 引脚被外部拉低，则该通道被关闭。在三相和四相应用中，所有相位的 FLT 引脚必须连接在一起，因此任何通道的故障都会导致所有其他通道的关闭。如果配置为故障后重新启动，则只有每个通道释放 FLT 引脚后，每个通道才会重新启动。

故障	VIN UV	OC	VOUT UV	VOUT OV	OT	OTFI
故障描述	输入电压高于 VIN_ON 阈值但低于 VIN_OFF 阈值	MOS 电流高于 过流故障阈值	FB 电压低于 UV 阈值	FB 电压高于 OV 阈值	MOS 温度高于 OT 阈值	IC 温度高于关断结温阈值
测量信号	Vin 电压	MOS 电流	FB 电压	FB 电压	MOS 温度	IC 温度
高侧 MOS	关断	关断	关断	关断	关断	关断
低侧 MOS	关断	关断	关断	导通	关断	关断
打嗝/锁存	无	取决于	取决于	锁存	温度低于恢复阈	温度低于恢复阈

		IOUT_OC_FAULT_RESPINSE	IOUT_OC_FAULT_RESPINSE		值后恢复	值后恢复
软启动之前	生效	失效	失效	固定 OV 阈值时生效，，跟踪 OV 阈值时失效	生效	生效
软启动之间	生效	逐周期限制	失效	固定 OV 阈值时生效，，跟踪 OV 阈值时失效	生效	生效
软启动之后	生效	生效	生效	生效	生效	生效

多相模式

KD12T-60A 模块可以配置为单相、两相、三相或四相输出。KD12T-60A 支持的工作模式如下表所示。

工作模式	模块	通道	
单相	单个模块	CH1 = 主机，，CH2 = 从机	
两相	单个模块	CH1 = 主机，，CH2 = 从机	
三相	两个模块	U1	CH1 = 主机，，CH2 = 从机 2
		U2	CH1 = 从机 1，CH2 = 独立通道
四相	两个模块	U1	CH1 = 主机，，CH2 = 从机 2
		U2	CH1 = 从机 1，CH2 = 从机 3

注意：

在多相工作时，从机的 FB 引脚必须与特定模块的 BP5 引脚相连接，各通道的 COMP 引脚需总线连接在一起，ISH 引脚需总线连接在一起，保证各通道间的电流共享。FLT 引脚需总线连接在一起，以确保所有通道在任何通道发生故障时关闭。还需确保 MFR_SPECIFIC_22 （PWM_OSC_SELECT） （E6h）命令被正确配置，以确保各通道相位之间的相移正确。

在三相和四相工作时，两个模块的 SYNC 引脚需总线连接在一起，两个模块的 PHSET 引脚需总线连接在一起，保证相间相移。

过温保护

PMBus 可配置过温故障和警告阈值，在过温故障的情况下，通道关闭高侧和低侧 MOS。当检测到的温度散热至低于阈值时，通道尝试重新启动。更多信息可以在 OT_FAULT_LIMIT 和 OT_WARN_LIMIT 命令描述中找到。

如果模块内部的 IC 结温达到关断阈值，PWM 输出信号被关闭。当结温散热到开启阈值时，PWM 重新启动，就像正常上电周期一样。

热设计

该产品可工作在不同的热环境下，但必须提供足够的散热以确保模块可靠运行。散热主要通过模块引脚到主板的热传导，以及流经模块的对流风速来实现。温度降额曲线提供了在特定 Vin 下的输出电流与环境温度和风速的关系。

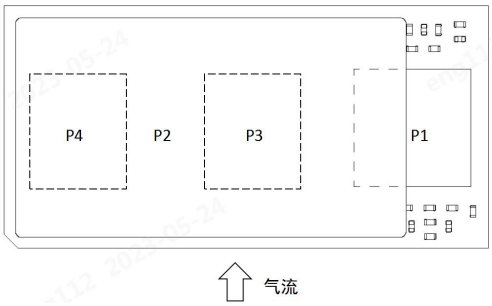
该模块在 254 x 254 mm，35μm，8 层 1 oz 测试板上测试，垂直安装在截面为 608 x 203 mm 的风洞中。另外请注意模块和主板之间连接的低阻抗可有效减少额外的功率损耗。

产品工作温度定义

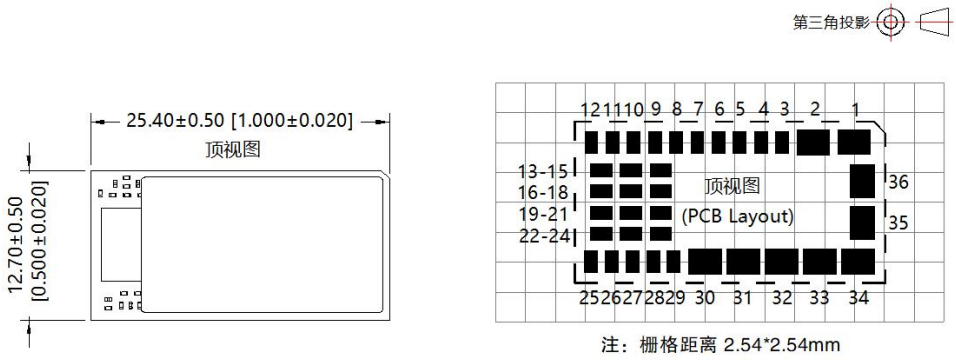
P1、P2、P3 和 P4 位置的表面温度不应超过下表中的最高温度，若超过最高温度可能会造成模块永久性损坏。

位置	描述	最高温度
P1	控制芯片	T_{P1} = 130℃
P2	功率电感	T_{P2} = 130℃
P3	MOS	T_{P3} = 130℃
P4	MOS	T_{P4} = 130℃

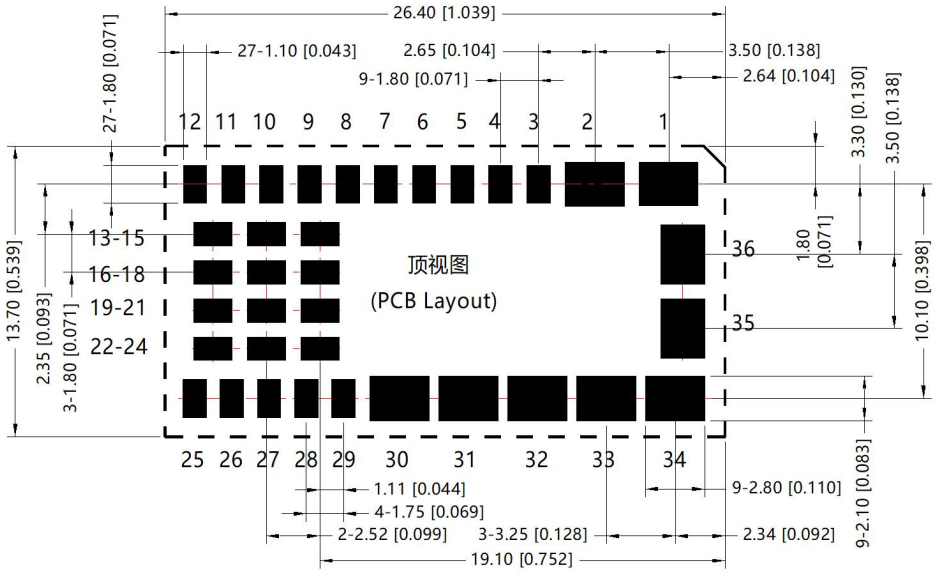
由于很难测量 P3 和 P4 的温度，因此可以仅测量 P2 温度来判断是否低于所限制的最高温度，也可以使用 PMBus 测量得到 P1/P3/P4 的温度值。



外观尺寸图

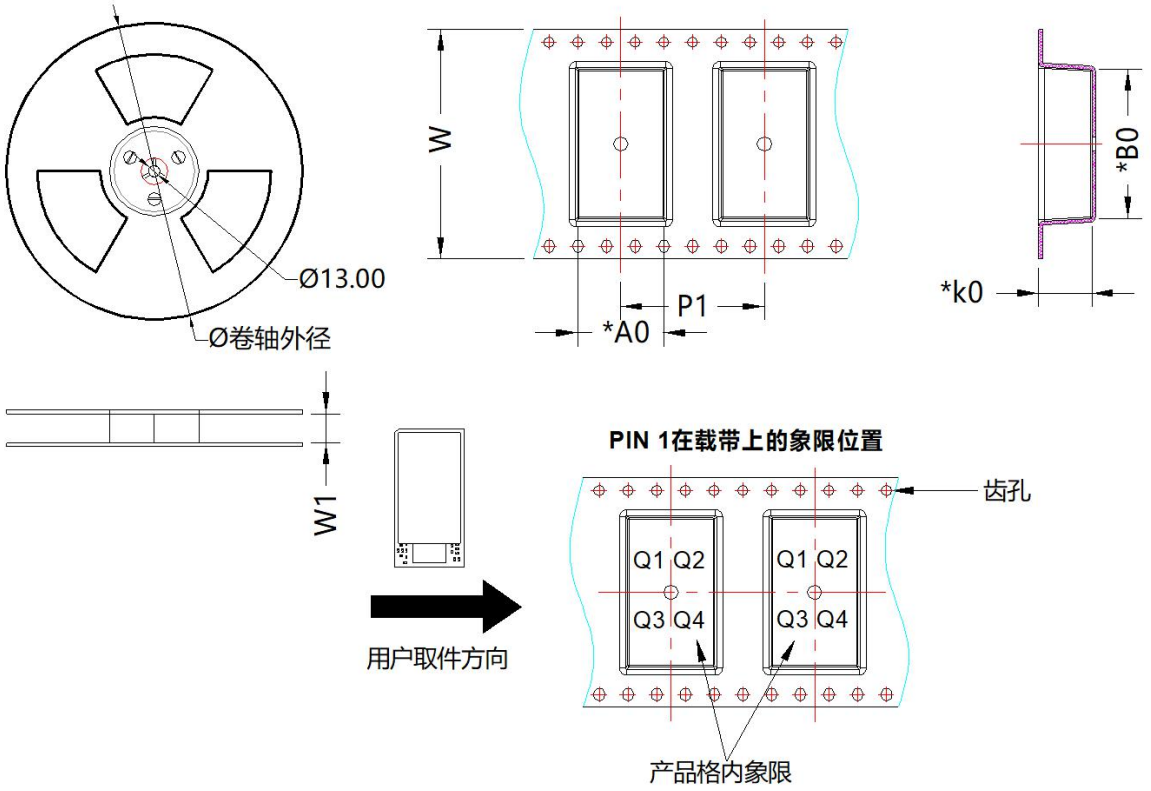


引脚方式			
引脚	功能	引脚	功能
1	Vin	19	BP5
2	GND	20	ADDR0
3	PG2	21	ISH2
4	PG1	22	FB2
5	CNTL2	23	FLT2
6	CNTL1	24	COMP2
7	SYNC	25	VSNS2
8	NC	26	GSNS2
9	ADDR1	27	FB1
10	PMBCLK	28	GSNS1
11	PMBDATA	29	VSNS1
12	SMBALERT	30	Vo2
13	AGND	31	Vo2
14	COMP1	32	GND
15	FLT1	33	Vo1
16	NC	34	Vo1
17	PHSET	35	GND
18	ISH1	36	Vin



比例 2：1

载带包装示意图



器件型号	封装类型	Pin	SPQ	卷轴外径 (mm)	卷轴宽度 W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 象限
KD12T-60A	SMD	36	160	330.0	44.4	14.08	26.58	14.26	24	44	Q1

PMBus 寄存器

CODE	COMMAND NAME	WORD/BYTE	DESCRIPTION: PMBus Command	USER WRITABLE	FACTORY DEFAULT VALUE
00h	PAGE	Byte	Locates separate PMBus command lists in multiple output environments	YES	0XXX XXX0
01h	OPERATION	Byte	Turn the unit on and off in conjunction with the input from the CONTROL pin. Set the output voltage to the upper or lower MARGIN VOLTAGES.	YES	0X00 00XX
02h	ON_OFF_CONFIG	Byte	Configures the combination of CONTROL pin input and serial bus commands needed to turn the unit on and off. This includes how the unit responds when power is applied.	YES	XXX1 0110
03h	CLEAR_FAULTS	Byte	Clears all fault status registers to 0x00. The "Unit is Off" bit in the status byte is not cleared when this command is issued.	YES[1]	NONE
10h	WRITE_PROTECT	Byte	Prevents unwanted writes to the device.	YES	000X XXXX
15h	STORE_USER_ALL	Byte	Saves the current configuration into the User Store. Note: This command writes to Non-Volatile Memory.	YES[1]	NONE
16h	RESTORE_USER_ALL	Byte	Restores Store. all parameters to the settings saved in the User	YES[1]	NONE
19h	CAPABILITY	Byte	PEC,SPD,ALRT	No	1011 0000
20h	VOUT_MODE	Byte	Read-Only Mode Indicator. The data format is linear with an exponent of -9	No	0001 0111
35h	VIN_ON	Word	Sets the value of the input voltage at which the unit should start power conversion	YES	1111 0000 0001 1001
36h	VIN_OFF	Word	Sets the value of the input voltage at which the unit should stop power conversion.	YES	1111 0000 0001 1000

38h	IOUT_CAL_GAIN	Word	Sets the ratio of the voltage at the current sense pins to the sensed current.	YES	1000 0000 0010 0001
39h	IOUT_CAL_OFFSET	Word	Nulls any offsets in the output current sensing circuit	YES	1110 0000 0000 0000
46h	IOUT_OC_FAULT_LIMIT	Word	Sets the value of the output current, in amperes, that causes the over-current detector to indicate an over-current fault condition.	YES	1111 1000 0110 0100
47h	IOUT_OC_FAULT_RESPONSE	Byte	Instructs the device on what action to take in response to an output over-current fault.	YES	0000 0111
4Ah	IOUT_OC_WARN_LIMIT	Word	Sets the value of the output current that causes an output Over-current warning	YES	1111 1000 0110 0010
4Fh	OT_FAULT_LIMIT	Word	Over temperature fault threshold	YES	0000 0000 1010 0101
5Ih	OT_WARN_LIMIT	Word	Over temperature warning threshold	YES	0000 0000 1000 1100
61h	TON_RISE	Word	Target soft-start rise time	YES	1110 0000 0010 1011
78h	STATUS_BYTE	Byte	Single byte status indicator	No	0x00 0000
79h	STATUS_WORD	Word	Full 2-byte status indicator	No	0000 0000 0x00 0000
7Ah	STATUS_VOUT	Byte	Output voltage fault status detail	No	0000 0000
7Bh	STATUS_IOUT	Byte	Output current fault status detail	No	0000 0000
7Dh	STATUS_TEMPERATURE	Byte	Temperature fault status detail	No	0000 0000
7Eh	STATUS_CML	Byte	Communication, memory, and logic fault status detail	No	0000 0000
80h	STATUS_MFR_SPECIFIC	Byte	Manufacturer specific fault status detail	No	0000 0000
8Bh	READ_VOUT	Word	Read output voltage	No	0000 0000 0000 0000
8Ch	READ_IOUT	Word	Read output current	No	1110 0000 0000 0000
8Eh	READ_TEMPERATURE_2	Word	Read off-chip temp sensor	No	1111 0000 0110 0100
98h	PMBUS_REVISION	Byte	PMBus Revision Information	No	0001 0001
D0h	MFR_SPECIFIC_00	Word	User scratch pad	YES	0000 0000 0000 0000
D4h	MFR_SPECIFIC_04	Word	VREF_TRIM	YES	0000 0000 0000 0000
D5h	MFR_SPECIFIC_05	Word	STEP_VREF_MARGIN_HIGH	YES	0000 0000 0001 1110
D6h	MFR_SPECIFIC_06	Word	STEP_VREF_MARGIN_LOW	YES	1111 1111 1110 0010

D7h	MFR_SPECIFIC_07	Byte	PCT_VOUT_FAULT_PG_LIMIT	YES	XXXX XX10
D8h	MFR_SPECIFIC_08	Byte	SWQUENCE_TON_TOFF_DELAY	YES	000X 000X
E0h	MFR_SPECIFIC_16	Word	COMM_EEPROM_SPARE	YES	1011 0001 xxxx x011
E5h	MFR_SPECIFIC_21	Word	IC options	YES	0111 1111 0000 0000
E6h	MFR_SPECIFIC_22	Word	PWM_OSC_SELECT	YES	0000 0000 0000 0000
E7h	MFR_SPECIFIC_23	Word	Paged and Common MASK_SMBALERT	YES	0000 0000 0000 0000
EFh	MFR_SPECIFIC_30	Word	Temperature offset	YES	1111 1000 0000 0000
FCh	MFR_SPECIFIC_44	Word	Device code, unique code to id part number	No	0000 0001 1110 0000

NOTE 1：No data bytes are sent, only the command code is sent.

PAGE (00h)

Format	Unsigned binary integer
Description	The PAGE command provides the ability to configure, control, and monitor through only one physical address both channels (outputs) of the device.
Default	0XXX XXX0 (binary)

PAGE							
r/w	r	r	r	r	r	r	r/w
7	6	5	4	3	2	1	0
PA	X	X	X	X	X	X	P0

Bits	Field Name	Description
7,0	PA,P0	00: (Default) All commands address the first channel. 01: All commands address the second channel. 10: Illegal input-ignore this write, take no action. 11: All commands address both channels. If PAGE = 11, any then read commands point to PAGE0 always.
6:1	X	X indicates writes are ignored and reads are 0. Any values written to read-only registers are ignored.

OPERATION (01h)

Format	Unsigned binary integer
Description	The OPERATION command is used to turn the device output on or off in conjunction with the input from the CNTLx pin (where x = 1 for channel 1 and x = 2 for channel 2). It is also used to set the output voltage to the upper or lower MARGIN levels. OPERATION is a paged register. In order to access OPERATION register for channel 1 of the device, PAGE must be set to 0. In order to access OPERATION register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command are ignored. An attempt to read and write the SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	0X0000XX (binary)

r/w	r	r/w	r/w	r/w	r/w	r	r
7	6	5	4	3	2	1	0
On	0	Margin				X	X

Bits	Field Name	Description
7	On	The On bit is used to enable to IC via PMBus. The necessary condition for this bit to be effective is that the cmd bit in the ON_OFF CONFIG register is set high. However, the cmd bit being high is not a sufficient condition to enable the IC via the On bit, as specified below: 0: (Default) The device output is not enabled via PMBus. 1: The device output is enabled if: a. The supply voltage VIN is greater than the VIN_UVLO threshold, the cmd bit is high, and b. The bit cpr in the ON_OFF CONFIG register is low, or c. The bit cpr is high and the CNTL_EN pin is enabled (high or low).
6	0	X: Default
5:2	Margin	If Margin Low is enabled, load the value from the STEP_VREF_MARGIN_LOW command. If Margin High is enabled, load the value from the STEP_VREF_MARGIN_HIGH command. (See PMBus specification for more information) 0000: (Default) Margin Off 0101: Margin Low (Ignore Fault) 0110: Margin Low (Act On Fault) 1001: Margin High (Ignore Fault) 1010: Margin High (Act On Fault) Note: Any values written to read-only registers are ignored.
1:0	X	XX: Default X indicates writes are ignored and reads are 0. Any values written to read-only registers are ignored.

ON_OFF_CONFIG (02h)

Format	Unsigned binary integer
Description	The ON_OFF_CONFIG command configures the combination of CONTROL pin input and serial bus commands needed to turn the unit on and off. ON_OFF_CONFIG is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device , PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11.If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command are ignored. An attempt to read and write the SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT. However, note that page 0 (channel 1) fault status bits (and associated smbalert state) should be capable of being cleared by toggling CNTL1 pin even if channel 1 is a slave. If channel 2 is a slave, then CNTL2 pin is disabled but toggling the CNTL1 pin should also clear page 1 (channel 2) fault status bits and related smbalert state. (The is recommendation is to tie together CNTL1 pins of both devices in a multi-phase configuration).
Default	XXX10110 (binary) The default power-up state can be changed using the STORE_USER_ALL command.

			r/w^E	r/w^E	r/w^E	r/w^E	r
7	6	5	4	3	2	1	0
X	X	X	pu	cmd	cpr	pol	cpa

Bits	Field Name	Description
7:5	X	X indicates writes are ignored and reads are 0.
4	pu	(Format: binary) Sets the default to either operate any time power is present or for the on/off to be controlled by CONTROL pin and/or PMBus commands. This bit is used in conjunction with the 'cp', 'cmd', and 'on' bits to determine start up. 0: Device powers up any time power is present regardless of state of the CONTROL pin.

		1: (Default) Device does not power up until commanded by the CNTL_EN pin and/or OPERATION command as programmed in bits (3:0) of the ON_OFF_CONFIG register.
3	cmd	(Format: binary) The cmd bit controls how the device responds to commands received via the serial PMBus. This bit is used in conjunction with the 'cpr', 'pu', and 'on' bits to determine start up. 0: (Default) Device ignores the on bit in the OPERATION command. 1: Device responds to the on bit in the OPERATION command, as explained above.
2	cpr	(Format: binary) Set the CNTL_EN pin response. This bit is used in conjunction with the 'cmd', 'pu', and 'on' bits to determine start up. The cpr bit being high is a necessary but not sufficient condition to enable the IC via the CNTL_EN pin: 0: Device ignores the CNTL_EN pin, i.e., on/off is controlled only by the OPERATION command 1: (Default) The device output is enabled if: a. The supply voltage VIN is greater than the VIN_UVLO threshold, and the CNTL_EN pin is active (high or low), and b. The bit cmd in the ON_OFF CONFIG register is low, or c. The bit cmd is high and the bit on in the OPERATION register is high.
1	pol	(Format: binary) Polarity of the CONTROL pin 1: (Default) CONTROL pin is active high 0: CONTROL pin is active low To change this value, the user must change this value in the register, save it to the EEPROM and then reboot the device via power down for the new value to take effect.
0	cpa	(Format: binary) Sets CONTROL pin action when commanding the unit to turn off. 0: (Default) Use the programmed turn-off delay. Note: Any values written to read-only registers are ignored on write and returns a'0'when read.

CLEAR_FAULTS (03h)

Format	N/A
Description	CLEAR_FAULTS is a paged command. In order to issue this command for channel 1 of the device, PAGE must be set to 0. In order to issue this command for channel 2 of the device , PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command simultaneously clears all bits in all status registers in the selected PAGE. At the same time, the device negates (clears, releases) its SMB_ALERT signal output if the device is asserting the SMB_ALERT signal. The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart. If the fault is still present when the bit is cleared, the fault bit shall immediately be set again and the host notified by the usual means.

Bits	Field Name	Description
7:0		No data bytes are sent, only the command code is sent.

WRITE_PROTECT (10h)

Format	N/A

Description	The WRITE_PROTECT command is used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to a device's configuration or operation. All supported commands may have their parameters read, regardless of the WRITE_PROTECT settings. Note: Valid setting of WRITE_PROTECT(7:5) bits disables the RESTORE_USER_ALL command's ability to restore EEPROM data to protected PMBus Control/Status Registers (CSRs). However, an EEPROM (via the RESTORE_USER_ALL execution) restores the data to any registers the remain unprotected (either by a valid WRITE_PROTECT(7:5) setting, or by any invalid setting of these bits). No WRITE_PROTECT(7:5) bit setting affects the Reset-Restore operation. All registers having EEPROM support get updated. Likewise, STORE_USER_ALL command operation remains unaffected.
Default	000XXXXX (binary) The default power-up state can be changed using the STORE_USER_ALL command.

r/w^E	r/w^E	r/w^E					
7	6	5	4	3	2	1	0
bit7	bit6	bit5	X	X	X	X	X

Bits	Field Name	Description
7	bit7	(Format: binary) 0: (Default) See table below. 1: Disable all writes except for the WRITE_PROTECT command. (bit5 and bit6 must be 0 to be valid data)
6	Bit6	(Format: binary) 0: (Default) See table below. 1: Disable all writes except for the WRITE_PROTECT, OPERATION, and PAGE commands. (bit5 and bit7 must be 0 to be valid data)
5	Bit5	(Format: binary) 0: (Default) See table below. 1: Disable all writes except for the WRITE_PROTECT, OPERATION, PAGE, and ON_OFF_CONFIG commands. (bit6 and bit7 must be 0 to be valid data)
4:0	X	X indicates writes are ignored and reads are 0. Note: Any values written to read-only registers are ignored.
Invalid data written to WRITE_PROTECT(7:5) causes the cml bit in the STATUS_BYTE and the ivd bit in the STATUS_CML registers to be set. INVALID DATA ALSO RESULTS IN NO WRITE PROTECTION (WRITE_PROTECT = 00h)!		

Data Byte Value	Action
1000 0000	Disables all WRITES except to the WRITE_PROTECT command.
0100 0000	Disables all WRITES except to the WRITE_PROTECT, OPERATION, and PAGE commands.
0010 0000	Disables all WRITES except to the WRITE_PROTECT, OPERATION, PAGE, and ON_OFF_CONFIG commands.

STORE_USER_ALL (15h)

Format	N/A
Description	Store all of the current storable register settings in the EEPROM memory as the new defaults on power up. It is permitted to use the STORE_USER_ALL command while the device is operating. However, the device may be unresponsive during the write operation with unpredictable memory storage results. It is recommended to turn the device output off before issuing this command. EEPROM programming faults set the cml bit in the STATUS_BYTE and the oth bit in the STATUS_CML registers.

RESTORE_USER_ALL (16h)

Format	N/A
Description	Write EEPROM data to those registers which: (1) have EEPROM support, and; (2) are unprotected according to current setting of the WRITE_PROTECT(7:5) bits. It is permitted to use the RESTORE_USER_ALL command while the device is operating. However, the device may be unresponsive during the copy operation with unpredictable, undesirable or even catastrophic results. It is recommended to turn the device output off before issuing this command.

Bits	Field Name	Description
7:0		No data bytes are sent, only the command code is sent.

CAPABILITY (19h)

Format	N/A
Description	This command provides a way for a host system to determine some key capabilities of this PMBus device.
Default	10110000 (binary)

r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0
PEC	SPD		ALRT	Reserved			

Bits	Field Name	Description
7	PEC	(Format: binary) Packet Error Checking is supported. 1: Default Note: Any values written to read-only registers are ignored.
6:5	SPD	(Format: binary) Maximum supported bus speed is 400 kHz. 01: Default Note: Any values written to read-only registers are ignored.
4	ALRT	(Format: binary) This device does have a SMB_ALERT pin and does support the SMBus Alert Response Protocol. 1: Default Note: Any values written to read-only registers are ignored.

3:0	Reserved	Reserved bits. 0000: Default

VOUT_MODE (20h)

Format	N/A
Description	The PMBus specification dictates that the data word for the VOUT_MODE command is one byte that consists of a 3-bit Mode and 5-bit parameter, as shown below. If a host sends a VOUT_MODE writer command, the device rejects the VOUT_MODE command, declare a communication fault for invalid data and respond as described in PMBus specification II section 10.2.2.
Default	00010111 (binary)

r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0
Mode			Exponent				

Bits	Field Name	Description
7:5	Mode	(Format: binary) 000: (Default) Linear Format
4:0	Exponent	(Format: two's complement binary) 10111: (Default) Exponent value =–9 Note: Any values written to read-only registers are ignored.

VIN_ON (35h)

The VIN_ON command sets the value of the input voltage at which the unit should start power conversion assuming all other conditions are met.

Values written within the supported VIN range are mapped to the nearest supported increment.

The supported VIN_ON values are:

4.25	4.5	4.75	5	5.25	5.5	5.75
6	6.25 (default)	6.5	6.75	7	7.25	7.5
7.75	8	8.25	8.5	8.75	9	9.25
9.5	10	10.5	11	11.5	12	12.5
13	14	15	16			

Format	Linear
Description	Attempts to write values outside of the acceptable range are treated as invalid data–in effect, the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML register are set, and SMB_ALERT asserted. Additionally, the value of VIN_ON remains unchanged. Maintaining values within "acceptable range" also indicates that writes to VIN_ON should not attempt to set its value less than that of VIN_OFF.
Default	The default setting results in a real VIN_ON of 6.25 V The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's complement) This is the exponent for the linear format. Default: 11110 (bin) –2 (dec) (equivalent LSB = 0.25 V) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's complement) This is the Mantissa for the linear format. Default: 000 0001 1001 (bin) 17 (dec) (equivalent VIN_ON voltage = 6.25 V) Minimum: 000 0001 0001 (bin) 17 (dec) (equivalent VIN_ON voltage = 4.25 V) Maximum: 000 0100 0000 (bin) 64 (dec) (equivalent VIN_ON voltage = 16 V) Note: Any values written to read-only registers are ignored

VIN_OFF (36h)

The VIN_OFF command sets the value of the input voltage at which the unit should stop power conversion.

Values written within the supported VIN range are mapped to the nearest supported increment.

The supported VIN_ON values are:

4 (default)	4.25	4.5	4.75	5	5.25	5.5
5.75	6 (default)	6.25	6.5	6.75	7	7.25
7.5	7.75	8	8.25	8.5	8.75	9
9.25	9.75	10.25	10.75	11.25	11.75	12.25
12.75	13.75	14.75	15.75			

Format	Linear
Description	Attempts to write values outside of the acceptable range are treated as invalid data – in effect, the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML register are set, and SMB_ALERT asserted. Additionally, the value of VIN_OFF remains unchanged. Maintaining values within "acceptable range" also indicates that writes to VIN_OFF should not attempt to set its value equal to or higher than that of VIN_ON.
Default	The default setting results in a real VIN_OFF of 6 V The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's complement) This is the exponent for the linear format.

		Default: 11110 (bin) –2 (dec) These default settings are not programmable. Note: Any values written to read-only registers are ignored
2:0 7:0	Mantissa	(Format: two's complement) This is the linear format Mantissa. Default: 000 0001 1000 (bin) 16 (dec) (equivalent VIN_OFF voltage = 6 V) Minimum: 000 0001 0000 (bin) 16 (dec) (equivalent VIN_OFF voltage = 4 V) Maximum: 000 0011 1111 (bin) 63 (dec) (equivalent VIN_OFF voltage = 15.75 V) Note: Any values written to read-only registers are ignored.

IOUT_CAL_GAIN (38h)

Format	Linear
Description	The IOUT_CAL_GAIN is the ratio of the voltage at the current sense element to the sensed current. The units are ohms. The effective current sense element is the DCR of the inductor. The default setting is 0.5 mΩ. The resolution is 15.26 μΩ. The range is 0.244 to 7.747 mΩ. The IOUT_CAL_GAIN needs to be set to 0.5 mΩ for correct current readout. With regards to multi-phase operation: The user can always write to PAGE 0 (channel 1), PAGE 1 (channel 2) can be written only if it is a master (in effect, the user can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE 0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT. IOUT_CAL_GAIN is a paged register. In order to access this register for channel 1 of the device, PAGE(7),(0) must be set to 00. In order to access this register for channel 2 of the device , PAGE(7),(0) must be set to 01. For simultaneous access of channels 1 and 2, PAGE(7),(0) command must be set to 11
Default	The default setting results in a real IOUT_CAL_GAIN of 0.5035 mΩ. The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's complement) This is the exponent for the linear format. Default: 10000 (bin)–16 (dec) (15.26 μΩ) These default settings are not programmable. Note: Any values written to read-only registers are ignored.

2:0 7:0	Mantissa	(Format: two's complement) This is the linear format Mantissa. Default: 000 0010 0001 (bin) 32 (dec) (32x15.26 μΩ = 0.5035 mΩ) Minimum 016 (dec) = 16x15.26 μΩ = 0.244 mΩ Maximum 508 (dec) = 508x 15.26 μΩ = 7.747 mΩ Note: Any values written to read-only registers are ignored.

IOUT_CAL_OFFSET (39h)

Format	Linear
Description	The IOUT_CAL_OFFSET is used to compensate for offset errors in the READ_IOUT command, the IOUT_OC_FAULT_LIMIT command and the IOUT_OC_WARN_LIMIT command. The units are amps. The default setting is 0 A. The resolution is 62.5 mA. The range is 3.9375 A to -4 A. Values outside the valid range are not checked and become aliased into the valid range. For example, 1110 0100 0000 0001 has an expected value of–63.9375 A but results in 1110 0111 1111 0001 which is–3.9375 A. This change occurs because the read-only bits are fixed. The exponent is always –4 and the 5 msb bits of the mantissa are always equal to the sign bit. IOUT_CAL_OFFSET is a paged register. In order to access this register for channel 1 of the device, PAGE(7),(0) must be set to 00. In order to access this register for channel 2 of the controller, PAGE(7),(0) must be set to 01. For simultaneous access of channels 1 and 2, PAGE(7),(0) command must be set to 11. With regards to multi-phase operation: The user can always write to PAGE 0 (channel 1). PAGE 1 (channel 2) can be written only if it is a master (i.e. the user can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value are used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r/w^E	r*	r*	r*	r*	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's complement) This is the exponent for the linear format. Default: 11100 (bin) –4 (dec) (lsb = 62.5 mA) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's complement) This is the linear format Mantissa. This is the linear format Mantissa. Default: 0 (bin) 0 (dec) Bits 1:0, and 7:6 changes for sign extension but are not otherwise programmable Note: Any values written to read-only registers are ignored.

IOUT_OC_FAULT_LIMIT (46h)

Format	Literal
Description	The IOUT_OC_FAULT_LIMIT command sets the value of the output current, in amperes, that causes the overcurrent detector to indicate an over-current fault condition. The IOUT_OC_FAULT_LIMIT should always be set to equal to or greater than the IOUT_OC_WARN_LIMIT. Writing a value to IOUT_OC_FAULT_LIMIT less than IOUT_OC_WARN_LIMIT causes the device to set the 'cml' bit in the STATUS_BYTE register and the 'ivd' bit in the STATUS_CML registers and assert SMB_ALERT. IOUT_OC_FAULT_LIMIT is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the controller, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. With regards to multi-phase operation: The user can always write to PAGE 0 (channel 1). PAGE 1 (channel 2) can be written only if it is a master (in effect, the user can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	1111 1000 0110 0100 (binary) The default setting results in a real IOUT_OC_FAULT_LIMIT of 50 A. The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's complement) This is the exponent for the linear format. Default: 11111 (bin) -1 (dec) (0.5 A) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's complement) Default: 000 0110 0100 (bin) 100 (dec) (equivalent analog OC = 50 A) Minimum: 000 0000 0110 (bin) 6 (dec) (equivalent analog OC = 3 A) Maximum: 000 0110 0100 (bin) 100 (dec) (equivalent analog OC = 50 A) Note: Any values written to read-only registers are ignored.

IOUT_OC_FAULT_RESPONSE (47h)

Format	Unsigned binary
Description	The IOUT_OC_FAULT_RESPONSE command instructs the device on what action to take in response to an IOUT_OC_FAULT_LIMIT or a VOUT under-voltage (UV) fault. When an OC fault is triggered, the device also: • Sets the OCF bit in the STATUS_BYTE register

	• Sets the OCFW and OCF bits in the STATUS_WORD register • Sets the OCF and OCW bits in the STATUS_IOUT register • Asserts SMB_ALERT, and notifies the host as described in section 10.2.2 of the PMBus Specification. Bits (2:0) are hard-wired to 0x7 (3'b111) to indicate the 7xSoft-start time delay units in response to an over current or Vout undervoltage fault. IOUT_OC_FAULT_RESPONSE is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device , PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. With regards to multi-phase operation: The user can always write to PAGE 0 (channel 1). PAGE 1 (channel 2) can be written only if it is a master (in effect, the user can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 (channel 2) SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	00000111 (binary) The default power-up state can be changed using the STORE_USER commands.

r	r	r/wE	r/wE	r/wE	r	r	r
7	6	5	4	3	2	1	0
0	0	RS(2)	RS(1)	RS(0)	1	1	1

Bits	Field Name	Description
7:6	0	Default: XX (X indicates writes are ignored and reads are 0) Note: Any values written to read-only registers are ignored.
5:3	RS(2:0)	(Format: binary) Output over current retry setting 000: (Default) A zero value for the Retry Setting indicates that the unit does not attempt to restart. The output remains disabled until the fault is cleared (See section 10.7 of the PMBus spec.). 111: A one value for the Retry Setting indicates that the unit goes through a normal startup (Wait → SoftStart) continuously, without limitation, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown. Any value other than 000 or 111 is not accepted, such and attempt causes the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML register to be set, and SMB_ALERT to be asserted.
2:0	1	Default: xxx (x indicates writes are ignored and reads are 1) Note: Any values written to read-only registers are ignored.

IOUT_OC_WARN_LIMIT (4Ah)

Format	Literal (5-bit two's complement exponent, 11-bit two's complement mantissa)
Description	The IOUT_OC_WARN_LIMIT command sets the value of the output current, in amperes, that causes the over-current

	detector to indicate an over-current warning condition by setting the OCW in bit-5 of the STATUS_IOUT register. • Sets the OTHER bit in the STATUS_BYTE register • Sets the OCFW bit in the STATUS_WORD register • Set the OCW bit in the STATUS_IOUT register • Notifies the host (Asserts SMB_ALERT) IOUT_OC_WARN_LIMIT is a paged register. In order to access this register for channel 1 of the K12DT-60A device, PAGE must be set to 0. In order to access this register for channel 2 of the K12DT-60A controller, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. With regards to multi-phase operation: PAGE 0 can always be written to. PAGE 1 can be written only if it is a master (in effect, you can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT. The IOUT_OC_WARN_LIMIT should always be set to less than or equal to the IOUT_OC_FAULT_LIMIT. Writing a value to IOUT_OC_WARN_LIMIT greater than IOUT_OC_FAULT_LIMIT causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers and assert SMB_ALERT.
Default	1111 1000 0110 0010 (binary) The default setting results in a real IOUT_OC_WARN_LIMIT of 49 A. The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's complement) This is the exponent for the linear format. Default: 11111 (bin) –1 (dec) (0.5 A) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's complement) This is the Mantissa for the linear format. Output over current retry setting Default: 000 0110 0010 (bin) 98 (dec) (equivalent analog OC = 49 A) Minimum: 000 0000 0100 (bin) 4 (dec) (equivalent analog OC = 2 A) Maximum: 000 0110 0010 (bin) 98 (dec) (equivalent analog OC = 49 A) Note: Any values written to read-only registers are ignored.

OT_FAULT_LIMIT (4Fh)

Format	Literal (5-bit two's complement exponent, 11-bit two's complement mantissa)
Description	The OT_FAULT_LIMIT command sets the value of the temperature limit, in degrees Celsius, that causes an over-temperature fault condition when the sensed temperature from the external sensor exceeds this limit. Upon triggering the over-temperature fault, the following actions are taken: • Set the OTFW bit in the STATUS_BYTE register and STATUS_WORD register • Set the OTF and OTW bits in the STATUS_TEMPERATURE register • Notify the host (Asserts SMB_ALERT) • Generate internal signal/s CHx_TSD that eventually shut down the gate drivers. OT_FAULT_LIMIT is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device , PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. With regards to multi-phase operation: PAGE 0 can always be written to. PAGE 1 can be written only if it is a master (in effect, you can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT. The OT_FAULT_LIMIT must always be greater than the OT_WARN_LIMIT. Writing a value to OT_FAULT_LIMIT less than or equal to OT_WARN_LIMIT causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers and assert SMB_ALERT.
Default	0000 0000 1010 0101 (binary) The default setting results in a real OT_FAULT_LIMIT of 165℃. The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's complement) This is the exponent for the linear format. Default: 00000 (bin) 0 (dec) (represents mantissa with steps of 1℃) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's complement) This is the Mantissa for the linear format. Default: 000 1010 0101 (bin) 165 (dec) (165℃) Minimum: 000 0111 1000 (bin) 120 (dec) (120℃) Maximum: 000 1010 0101 (bin) 165 (dec) (165℃) Note: Any values written to read-only registers are ignored.

Table. OT_FAULT THRESHOLD Settings

TEMPERATURE (℃)(1)	OT_FAULT_THRESHOLD (℃ BIN)	TEMPERATURE (℃)	OT_FAULT RESET THRESHOLD (℃ BIN)
120	01111000	100	01100100
125	01111101	105	01101001
130	10000010	110	01101110
135	10000111	115	01110011
140	10001100	120	01111000
145	10010001	125	01111101
150	10010110	130	10000010
155	10011011	135	10000111
160	10100000	140	10001100
165	10100101	145	10010001

(1) Lists only multiples of 5℃; but, the actual LSB is 1℃.

OT_WARN_LIMIT (5Ih)

Format	Literal (5-bit two's complement exponent, 11-bit two's complement mantissa)
Description	The OT_WARN_LIMIT command sets the value of the temperature, in degrees Celcius, which causes an over-temperature warning condition. • Sets the OTFW bit in the STATUS_BYTE register and STATUS_WORD register • Sets the OTW bit in the STATUS_TEMPERATURE register • Notifies the host (Asserts SMB_ALERT) OT_WARN_LIMIT is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. With regards to multi-phase operation: PAGE 0 can always be written to. PAGE 1 can be written only if it is a master (in effect, you can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT. The OT_WARN_LIMIT should always be set to less than the OT_FAULT_LIMIT. Writing a value to OT_WARN_LIMIT greater than OT_FAULT_LIMIT causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers and assert SMB_ALERT.
Default	0000 0000 1000 1100 (binary) The default setting results in a real OT_WARN_LIMIT of 140℃. The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's complement) This is the exponent for the linear format. Default: 00000 (bin) 0 (dec) (1℃) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's complement) This is the Mantissa for the linear format. Default: 000 1000 1100 (bin) 140 (dec) (140℃) Minimum: 000 0110 0100 (bin) 100 (dec) (100℃) Maximum: 000 1000 1100 (bin) 140 (dec) (140℃) Note: Any values written to read-only registers are ignored.

Table. OT_WARN_LIMIT Settings

TEMPERATURE (℃)(1)	OT_FAULT_THRESHOLD (℃ BIN)	TEMPERATURE (℃)	OT_FAULT RESET THRESHOLD (℃ BIN)
100	01100100	80	1010000
105	01101001	85	1010101
110	01101110	90	1011010
115	01110011	95	1011111
120	01111000	100	1100100
125	01111101	105	1101001
130	10000010	110	1101110
135	10000111	115	1110011
140	10001100	120	1111000

(1) Lists only multiples of 5℃; but, the actual LSB is 1℃.

TON_RISE (61h)

Format	Linear
Description	The TON_RISE command sets the time in ms, from when the reference VREF starts to rise until it reaches the end value. It also determines the rate of transition of the reference VREF (either due to VREF_TRIM or STEP_VREF_MARGIN_HIGH/ STEP_VREF_MARGIN_LOW commands), when this transition is executed during the soft-start state. Values written within the supported range of TON_RISE are mapped to the nearest supported increment. TON_RISE is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. With regards to multi-phase operation: The user can always write to PAGE 0 (channel 1). PAGE 1 (channel 2) can be written only if it is a master (in effect, the user can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the

	user and can not be enforced by the hardware). An attempt to write a PAGE 1 (channel 2) SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	The default setting results in TON_RISE of 2.7ms The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's complement) This is the exponent for the linear format. Default: 11100 (bin) -4 (dec) (62.5 μs) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's complement) This is the Mantissa for the linear format. Default: 000 0010 1011 (bin) 43 (dec) (equivalent to 2.688 ms) Minimum: Any value equal or less than 12 dec is equivalent to the min 600 μs Maximum: Any value greater than 120 dec is equivalent to 9 ms Note: Any values written to read-only registers are ignored.

Table . Allowable TON_RISE Values

TON_RISE TIME (ms)	MANTISSA (BINARY)
0.6	000 0000 1010
0.9	000 0000 1110
1.2	000 0001 0011
1.8	000 0001 1101
2.7	000 0010 1011
4.2	000 0100 0011
6	000 0110 0000
9	000 1001 0000

STATUS_BYTE (78h)

Format	Unsigned binary
Description	The STATUS_BYTE command returns one byte of information with a summary of the most critical faults. STATUS_BYTE is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. If configured as a master, each channel indicates faults on its own channel. However, if configured as a slave, the output voltage faults – OVF, UVF, PGOOD are only be set for that slave's master (which may be in the other IC for 3-ph

	and 4-ph systems) while these faults for the slave are set to 0. Flags related to IOUT and TEMPERATURE (OCF, OCW, OTF, OTW) are set on PAGE 0 for channel 1 and PAGE 1 for channel 2, in all modes. The STATUS_BYTE register also reports communication faults in the Other Faults bit.
Default	0x000000 (binary)

7	6	5	4	3	2	1	0
0	OFF	OVF	OCF	VIN_UV	OTFW	cml	oth

Bits	Field Name	Description
7	0	Default: 0
6	OFF	(Format: binary) Output is OFF This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. 0: Unit is on 1: Unit is off
5	OVF	(= VOUT_OV in PMBus Specification) (Format: binary) Output Over-Voltage Fault Triggers SMB_ALERT. For a slave configuration, this bit is set to 0. 0: (Default) An output over-voltage fault has not occurred. 1: An output over-voltage fault has occurred.
4	OCF	(=IOUT_OC in PMBus Specification) (Format: binary) Output Over-Current Fault 0: (Default) An output over-current fault has not occurred. 1: An output over-current fault has occurred.
3	VIN_UV	(Format: binary) Input voltage (VIN) under-voltage fault. This bit is defined only on PAGE0. For PAGE1, this bit is 0. This bit is masked before soft-start is finished. 0: (Default) An input under-voltage fault has not occurred. 1: An input under-voltage fault has occurred.
2	OTFW	(= TEMPERATURE in PMBus Specification) (Format: binary) Over-Temperature Fault/warning OTF or OTW input has been asserted by the external sensor for that channel. 0: (Default) An over-temperature fault or warning has not occurred. 1: An over-temperature fault or warning has occurred.

1	cml	(= CML in PMBus Specification) (Format: binary) Communications, memory or logic fault has occurred. This bit is used to flag communications, memory or logic faults. 0: (Default) A communications, memory or logic fault has not occurred 1: A communications, memory or logic fault has occurred
0	oth	(= NONE OF THE ABOVE in the PMBus Specification) (Format: binary) Other Fault This bit is used to flag faults not covered with the other bit faults. In this case, UVF or OCW faults are examples of other faults not covered by the bits (7:1) in this register. 0: (Default) A fault or warning not listed in bits (7:1) has not occurred. 1: A fault or warning not listed in bits (7:1) has occurred.

STATUS_WORD (79h)

Format	Unsigned binary
Description	The STATUS_WORD command returns two bytes of information with a summary of the device's fault/warning conditions. STATUS_WORD is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. If PAGE command is set to 11, then PAGE 0 of the status register is read. The STATUS_WORD also reports a power good fault. If configured as a master, each channel indicates faults on its own channel. However, if configured as a slave, the output voltage faults (OVF, UVF, PGOOD) are be set only for that slave's master (which may be in the other device for 3-phase and 4-phase systems) while these faults for the slave are set to 0. Flags related to IOUT and TEMPERATURE (OCF, OCW, OTF, OTW) are set on PAGE 0 for channel 1 and PAGE 1 for channel 2, in all modes. The STATUS_WORD also reports communication faults in the Other Faults bit.
Default	000000000x000000 (binary)

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1
VF	OCFW	0	MFR	PGOOD_Z	0	0	0	0	OFF	OVF	OCF	VIN_UV	OTFW	cml

Bits	Field Name	Description
7	VF	(=VOUT in the PMBus Specification) (Format: binary) Voltage Fault = (OVF + UVF) For slave configurations, this bit is set to 0. 0: (Default) An output voltage fault or warning has not occurred. 1: An output voltage fault or warning has occurred.

6	OCFW	(= IOUT/POUT in the PMBus Specification) (Format: binary) Output Current Fault OR Warning = (OCF + OCW) 0: (Default) An output over-current fault or warning has not occurred. 1: An output over-current fault or warning has occurred.
5	0	Default: 0
4	MFR	(= MFR in the PMBus Specification) (Format: binary) Internal thermal fault (from bandgap) Thermal shutdown fault for the IC 0: (Default) An internal TSD has not occurred. 1: An internal TSD has occurred.
3	PGOOD_Z	(= POWER_GOOD# in the PMBus Specification) (Format: binary) Power Good Fault (in effect, Power Good Indication–Inverted) The Power Good fault is used to flag when the converter output voltage rises or falls outside of the PGOOD window. If the channel is configured as a slave, this bit are set to "0" (PGOOD_Z is only reflected in the master). 0: (Default) A Power Good fault is not present. 1: Device-channel experiencing a Power Good fault.
2:0	0	Default: 0

The STATUS_WORD low byte is the STATUS_BYTE.

STATUS_VOUT (7Ah)

Format	Unsigned binary
Description	The STATUS_VOUT command returns one byte of information relating to the status of the converter's output voltage related faults. The PMBus core is notified of these fault conditions via the 2 input pins labeled OVF and UVF. The PMBus core then communicates these faults to the host through its serial communication channel. STATUS_VOUT is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11.
Default	00000000 (binary)

7	6	5	4	3	2	1	0
OVF	0	0	UVF	0	0	0	0

Bits	Field Name	Description
7	OVF	(= VOUT OV Fault in the PMBus Specification) (Format: binary)

		Output Over-Voltage Fault Set based upon the value stored in MFR_SPECIFIC_07 (D7h). If the channel is configured as a slave this bit are set to 0 (this bit is only reflected in the master). 0: (Default) An output over-voltage fault has not occurred. 1: An output over-voltage fault has occurred.
6:5	0	Default: 0
4	UVF	(= VOUT UV Fault in the PMBus Specification) (Format: binary) Output Under-Voltage Fault Set based upon the value stored in MFR_SPECIFIC_07 (D7h). If the channel is configured as a slave this bit are set to 0 (this bit is only reflected in the master). The UV fault indicates only an under-voltage condition at the FB pin and may not necessarily reflect an over-current situation. However, during an output crowbar short condition, the FB may sag below the UV threshold level before the current reaches the OC threshold, resulting in a UV fault. If the IOUT_OC_FAULT_RESPONSE register is selected to the retry setting, and the output short is persistent, an over-current fault are triggered for subsequent start-up retry attempts. 0: (Default) An output under-voltage fault has not occurred. 1: An output under-voltage fault has occurred.
3:0	0	Default: 0

STATUS_IOUT (7Bh)

Format	Unsigned binary
Description	The STATUS_IOUT command returns one byte of information relating to the status of the converter's output current related faults. The PMBus core is notified of these fault conditions via the inputs OCF and OCW. STATUS_IOUT is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11.
Default	00000000 (binary)

7	6	5	4	3	2	1	0
OCF	0	OCW	0	0	0	0	0

Bits	Field Name	Description
7	OCF	(= IOUT OC Fault in the PMBus Specification) (Format: binary) Output Over-Current Fault Set based upon the value stored in IOUT_OC_FAULT_LIMIT 0: (Default) An output over-current fault has not occurred. 1: An output over-current fault has occurred.
6	0	Default: 0

5	OCW	(= IOUT OC Warning in the PMBus Specification) (Format: binary) Output Over-Current Warning Set based upon the value stored in IOUT_OC_WARN_LIMIT. 0: (Default) An output over-current warning has not occurred. 1: An output over-current warning has occurred.
4:0	0	Default: 0

STATUS_TEMPERATURE (7Dh)

Format	Unsigned binary
Description	The STATUS_ TEMPERATURE command returns one byte of information relating to the status of the converter's die temperature related faults. STATUS_TEMPERATURE is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11.
Default	00000000 (binary)

7	6	5	4	3	2	1	0
OTF	OTW	0	0	0	0	0	0

Bits	Field Name	Description
7	OTF	(= OT Fault in the PMBus Specification) (Format: binary) Over-Temperature Fault 0: (Default) A temperature fault has not occurred. 1: A temperature fault has occurred.
6	OTW	(= OT Warning in the PMBus Specification) (Format: binary) Over-Temperature Warning 0: (Default) A temperature warning has not occurred. 1: A temperature warning has occurred.
5:0	0	Default: 0

STATUS_CML (7Eh)

Format	Unsigned binary
Description	The STATUS_ CML command returns one byte containing PMBus serial communication faults.
Default	00000000 (binary)

7	6	5	4	3	2	1	0
ivc	ivd	pec	mem	0	0	oth	0

Bits	Field Name	Description
7	ivc	(= Invalid/Unsupported Command in the PMBus Specification) (Format: binary) Invalid or unsupported Command Received 0: (Default) Invalid or unsupported Command not Received. 1: Invalid or unsupported Command Received. An attempt to write an invalid PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
6	ivd	(= Invalid/Unsupported Data in the PMBus Specification) (Format: binary) Invalid or unsupported data Received 0: (Default) Invalid or unsupported data not Received. 1: Invalid or unsupported data Received.
5	pec	(= Packet Error Check Failed in the PMBus Specification) (Format: binary) Packet Error Check Failed This is a CRC byte sent at the end of each data packet. It is implemented as CRC(x) = x8 + x2 + x1 + 1 0: (Default) Packet Error Check Passed 1: Packet Error Check Failed
4	mem	(= Memory Fault Detected in the PMBus Specification) (Format: binary) Memory Fault Detected This bit indicates a fault with the internal memory. 0: (Default) No fault detected 1: Fault detected
3:2	0	Default: 0
1	oth	(= Other Communication Fault in the PMBus Specification) (Format: binary) Other Communication Fault 0: (Default) A communication fault other than the ones listed in this table has not occurred. 1: A communication fault other than the ones listed in this table has occurred.
0	0	Default: 0

STATUS_MFR_SPECIFIC (80h)

Format	Unsigned binary
Description	The STATUS_ MFR_SPECIFIC command returns one byte containing manufacturer-specific faults or warnings.

Default	00000000 (binary)

7	6	5	4	3	2	1	0
otfi	x	x	ivaddr	ch1_sps_flt	ch2_sps_flt	ch1_slave	ch2_slave

Bits	Field Name	Description
7	otfi	(Format: binary) Over temperature fault internal. This bit is required to distinguish an over temperature fault internal to the device from an external temperature fault. 0: (Default) The internal temperature is below the fault threshold. 1: The internal temperature is above the fault threshold.
6:5	x	Default: 0
4	ivaddr	(Format: binary) Invalid PMBus address This bit is set when the PMBus address detection circuit does not resolve to a valid address. In this event, the device responds to the address: 127d. 0: (Default)
3	ch1_sps_flt	(Format: binary) Channel 1 smart power-stage fault This bit reports that the smart power-stage has declared a fault (either over-current or over-temperature) . 0: (Default)
2	ch2_sps_flt	(Format: binary) Channel 2 smart power-stage fault This bit reports that the smart power-stage has declared a fault (either over-current or over-temperature) . 0: (Default)
1	ch1_slave	(Format: binary) Channel 1 Slave This bit is set when channel 1 is configured as a slave channel (by pulling FB1 > 2.5 V before power-up). It is only used for internal read purposes and does not trigger SMBLERT. 0: (Default)
0	ch2_slave	(Format: binary) Channel 2 Slave This bit is set when channel 2 is configured as a slave channel (by pulling FB2 > 2.5 V before power-up). It is only used for internal read purposes and does not trigger SMBLERT. 0: (Default)

READ_VOUT (8Bh)

Format	Linear
Description	The READ_VOUT command returns two bytes of data in the linear data format that represent the output voltage. The exponent is set to –9 by VOUT_MODE. VOUT = Mantissa x $2^{Exponent}$ READ_VOUT is a paged register. In order to access READ_VOUT register for channel 1 of the device, PAGE(7),(0) must be set to 00. In order to access READ_VOUT register for channel 2 of the device, PAGE(7),(0) must be set to 01. PAGE register cannot be set to 11 for READ_VOUT command.
Default	0000h

r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Mantissa															

Bits	Field Name	Description
7：0	Mantissa	(Format: unsigned binary) This is the Mantissa for the linear format. Default: 0000 0000 0000 0000 (bin) 0 (dec) Note: Any values written to read-only registers are ignored.

READ_IOUT (8Ch)

Format	Linear
Description	The READ_IOUT command returns the output current in amps for each channel. The reading from the Measurement System must be manipulated in order to convert the measured value into the desired value (IOUT). Note: only positive currents are reported. Any computed negative current (For example, 0 measured current and –4 A IOUT_CAL_OFFSET) is reported as 0 A. READ_IOUT is a paged register. In order to access READ_IOUT register for channel 1 of the device, PAGE(7),(0) must be set to 00. In order to access READ_IOUT register for channel 2 of the device, PAGE(7),(0) must be set to 01. PAGE(7),(0) register cannot be set to 11 for READ_IOUT command.
Default	E0000h

r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7：3	Exponent	(Format: two's complement) This is the exponent for the linear format. Default: 11100 (bin) -4 (dec) (62.5 mA lsb) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's complement) Default: 000 00000000 (bin) 0 (dec) Note: Any values written to read-only registers are ignored.

READ_TEMPERATURE_2 (8Eh)

Format	Linear
Description	The READ_TEMPERATURE_2 command returns the temperature in degrees Celsius of the current channel specified by the PAGE command.
Default	F064h

r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's complement) This is the exponent for the linear format. Default: 11110 (bin) –2 (dec) 0.25℃ These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's complement) Default: 000 0110 0100 (bin) 100 (dec) Note: Any values written to read-only registers are ignored.

PMBus_REVISION (98h)

Format	Linear
Description	The PMBus_REVISION command returns the revision of the PMBus to which the device is compliant. The device is compliant to revision 1.1 of the PMBus specification.
Default	00010001b

r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Bits	Field Name	Description
7:0	/	/

MFR_SPECIFIC_00 (D0h)

Format	Unsigned binary
Description	The MFR_SPECIFIC_00 register is dedicated as a user scratch pad
Default	0000h The default power-up state can be changed using the STORE_USER commands.

r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Bits	Field Name	Description
7:0		

MFR_SPECIFIC_04 (VREF_TRIM) (D4h)

Format	Linear
Description	The VREF_TRIM command is used to apply a fixed offset voltage to the reference voltage. VREF = 600 mV + (VREF_TRIM + STEP_VREF_MARGIN_x) x 2 mV The maximum trim range is 10% /–20% of nominal VREF (600 mV) in 2-mV steps. Permissible values are from 60 mV to–120 mV. Including settings from both VREF_TRIM and STEP_VREF_MARGIN_x commands, the net permissible range of VREF is 60 mV to–180 mV. If the commanded VREF_TRIM is outside its valid range, then that value is not accepted; it also causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers, and triggers SMB_ALERT. If the combined VREF set by VREF_TRIM and/or STEP_VREF_MARGIN_x is outside the acceptable range, it causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers, it triggers SMB_ALERT, and the VREF are set to the highest or lowest allowed value (based on the commanded level). The VREF transition occurs at the rate determined by the TON_RISE (61h) command if the transition is executed during soft-start. Any transition in VREF after soft-start occurs at the rate determined by the highest programmable TON_RISE of 9 ms. The VREF_TRIM has two data bytes formatted as two's complement binary integer and can have positive and negative values. If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command is ignored. (In analog, the master programmed value are used in a multi-phase system. No special action needed from digital.) An attempt to write the SLAVE channel command, or when in AVS mode results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	0000h (Fixed Offset Voltage = 0 V) The default power-up state can be changed using the STORE_USER commands.

r/w^E	r*	r*	r*	r*	r*	r*	r*	r*	r*	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Bits	Field Name	Description
7:0	High Byte	(Format: binary) Default: 0000 0000 (bin) Minimum: 1111 1111 (bin) (sign extended) Maximum: 0000 0000 (bin) (sign extended) Bits 6:0 changes for sign extension but are not otherwise programmable
7:0	Low Byte	(Format: binary) Default: 0000 0000 (bin) 0 (dec) 0 mV Minimum: 1100 0100 (bin) –60 (dec) (–120 mV) (sign extended, twos compliment) Maximum: 0001 1110 (bin) 30 (dec) (60 mV) Bits 7:6 changes for sign extension but are not otherwise programmable

MFR_SPECIFIC_05 (STEP_VREF_MARGIN_HIGH) (D5h)

Format	Linear
Description	The STEP_VREF_MARGIN_HIGH command is used to increase the value of the reference voltage by shifting the reference higher. When the OPERATION command is set to Margin High, the reference increases by the voltage (in mV) indicated by this command. Thus, the changed reference is given by: VREF = 600 mV + (VREF_TRIM + STEP_VREF_MARGIN_HIGH) x 2 mV The maximum range is 0 to 10% (60 mV) of nominal VREF (600 mV) in 2mV steps. Including settings from both VREF_TRIM and STEP_VREF_MARGIN_x commands, the net permissible range of VREF is 60 mV to −180 mV. If the commanded STEP_VREF_MARGIN_HIGH is outside its valid range, then that value is not accepted; it also causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers, and triggers SMB_ALERT. If the combined VREF set by VREF_TRIM and/or STEP_VREF_MARGIN_x is outside the acceptable range, it causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers, it triggers SMB_ALERT, and the VREF are set to the highest or lowest allowed value (based on the commanded level). The VREF transition occurs at the rate determined by the TON_RISE (61h) command if the transition is executed during soft-start. Any transition in VREF after soft-start occurs at the rate determined by the highest programmable TON_RISE of 9 ms. This is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command are ignored. (In analog, the master programmed value is used in a multi-phase system. No special action needed from digital). An attempt to write the SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	0000 0000 0001 1110 (binary) The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Bits	Field Name	Description
7:0	High Byte	(Format: binary) Default: 0000 0000 (bin) Minimum: 0000 0000 (bin) Maximum: 0000 0000 (bin) Note: Any values written to read-only registers are ignored.
7:0	Low Byte	(Format: binary) This specifies a positive offset voltage on to default VREF. Default: 0001 1110 (bin) 30 (dec) (60 mV = 10% percent) Minimum: 0000 0000 (bin) 0 (dec) (0 mV) Maximum: 0001 1110 (bin) 30 (dec) (60 mV = 10% percent)

MFR_SPECIFIC_06 (STEP_VREF_MARGIN_LOW) (D6h)

Format	Linear
Description	The STEP_VREF_MARGIN_LOW command is used to decrease the reference voltage by shifting the reference lower. When the OPERATION command is set to Margin Low, the output decreases by the voltage indicated by this command. Thus, the changed reference is given by: VREF = 600 mV + (VREF_TRIM + STEP_VOUT_MARGIN_LOW) x 2 mV .The maximum range is 0 to–20% (–120 mV) of nominal VREF (600 mV) in 2mV steps. Including settings from both VREF_TRIM and STEP_VREF_MARGIN_x commands, the net permissible range of VREF is 60 mV to–180 mV. If the commanded STEP_VREF_MARGIN_LOW is outside its valid range, then that value is not accepted; it also causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers, and triggers SMB_ALERT. If the combined VREF set by VREF_TRIM and/or STEP_VREF_MARGIN_x is outside the acceptable range, it causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers, it triggers SMB_ALERT, and the VREF is set to the highest or lowest allowed value (based on the commanded level). The VREF transition occurs at the rate determined by the TON_RISE (61h) command if the transition is executed during soft-start. Any transition in VREF after soft-start occurs at the rate determined by the highest programmable TON_RISE of 9 ms. This is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command are ignored. (In analog, the master programmed value is used in a multi-phase system. No special action needed from digital.) An attempt to write the SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	1111 1111 1110 0010 (binary) The default power-up state can be changed using the STORE_USER commands.

r/w^E	r*	r*	r*	r*	r*	r*	r*	r*	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Bits	Field Name	Description
7:0	High Byte	(Format: binary) Default: 1111 1111 (bin) (msb is sign bit) Minimum: 1111 1111 (bin) (sign extended) Maximum: 0000 0000 (bin) Bits 6:0 can change for sign extension but are not otherwise programmable
7:0	Low Byte	(Format: two's complement) This specifies a negative offset voltage on to default VREF. Default: 1110 0010 (bin) -30 (dec) (–60 mV = –10% percent) Minimum: 1100 0100 (bin) -60 (dec) (–120 mV = –20% percent) Maximum: 0000 0000 (bin) 0 (dec) (0 mV) Bits 7:6 can change for sign extension but are not otherwise programmable

MFR_SPECIFIC_07 (PCT_VOUT_FAULT_PG_LIMIT) (D7h)

Format	Unsigned binary integer
Description	The PCT_VOUT_FAULT_PG_LIMIT is to set the PGOOD, VOUT_UV and VOUT_OV limits. This is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command are ignored. (In analog, the master programmed value is used in a multi-phase system. No special action needed from digital.) An attempt to read and write the SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	XXXX XX10 (binary) The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	PG(1:0)

Bits	Field Name	Description
7:2	X	X indicates writes are ignored and reads are 0
1:0	PG(1:0)	(Format: binary) PG, UV, OV Limit Selection. Default: 10

Table lists the over-voltage, under-voltage, and power-good threshold voltages. Bit (13) of MFR_SPECIFIC_16 (E0h) register determines the overvoltage setting.

Table. OV, UV, PGOOD Threshold Values

PG(1)	PG(0)	UV_fault (%)	PG_low (%)	PG_high (%)	OV_fault (%)	OV_fault (mV)	OV SETTING
0	0	–16.8	–12.5	12.5	16.8	n/a	Tracking
0	1	–12.0	–7.0	7.0	12.0		
1	0	-29.0	–23.0	7.0	16.8		
1	1	–29.0	–23.0	7.0	12.0		
0	0	–16.8	–12.5	12.5	N/A	800	Fixed
0	1	–12.0	–7.0	7.0		700	
1	0	–29.0	–23.0	7.0		800	
1	1	–29.0	–23.0	7.0		700	

MFR_SPECIFIC_08 (SEQUENCE_TON_TOFF_DELAY) (D8h)

Format	Unsigned binary integer
Description	The SEQUENCE_TON_TOFF_DELAY command is used to set the delay for turning on the device and the delay for turning off the device as a ratio of TON_RISE. This is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command are ignored. In such a case, internally the TON_DELAY is set to the minimum value of 50 μs and TOFF_DELAY is set to zero (overriding any contents of EEPROM). An attempt to read and write the SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	000X 000X (binary) The default power-up state can be changed using the STORE_USER commands.

r/w^E	r/w^E	r/w^E	r	r/w^E	r/w^E	r/w^E	r
7	6	5	4	3	2	1	0
TON_DEL<2:0>			X	TOFF_DEL<2:0>			X

Bits	Field Name	Description
7:5	TON_DEL<2:0>	(Format: binary) Default: 000b TON_DELAY = TON_RISE x TON_DEL<2:0> This parameter controls the delay from when ON = 1 until soft-start sequence begins. The default value is 0 ms. (Start the VOUT ramp without delay)
4	X	X indicates writes are ignored and reads are 0
3:1	TOFF_DEL<2:0>	(Format: binary) Default: 000b TOFF_DELAY = TON_RISE x TOFF_DEL<2:0> This parameter controls the delay from when ON = 0 until the output is disabled. The default value is 0 ms. (Shut off the output without delay)
0	X	X indicates writes are ignored and reads are 0

Table . Delay Time Ratios

TON_DEL<2:0> TOFF_DEL<2:0>	DELAY TIME RATIO (MULTIPLE OF TON_RISE)
000	0
001	1
010	2

011	3
100	4
101	5
110	6
111	7

NOTE

If the device turns off due to a turn-off delay time, any attempt to turn on the device before the turn-off delay time expires should be avoided. The device is available to be turned on only after the turn-off delay time expires and the device has been turned off.

MFR_SPECIFIC_16 (COMM_EEPROM_SPARE) (E0h)

Format	Unsigned binary
Description	This register contains EEPROM backed bits brought out to the top of the digital block IO for possible future use by analog or digital circuits
Default	1011 0001 xxxx x011 (binary) The default power-up state can be changed using the STORE_USER commands.

COMM_EEPROM_SPARE							
r/w^E	r/w^E	r/w^E	r/w^E	r	r	r	r
15	14	13	12	11	10	9	8
PGOOD_DEL_EN	DIS_API_CNT	FIX_OVP_EN	DIS_SSPB				

COMM_EEPROM_SPARE							
r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0

Bits	Field Name	Description
15	PGOOD_DLY_EN	(format: binary, access: read/write) Default: 1b PGOOD Delay Enable This bit, when high, enable 2-ms delay for PGOOD detection during startup.
14	DIS_API_CNT	(format: binary, access: read/write) Default: 0b Disables 3-clock count for API valley active state This bit, when high, disables the 3-clock counter for API valley. When the bit is low, the counting is enabled whereby the API-valley function can remain active only 3 consecutive clock cycles before being inactive for another 3 clocks.

13	FIX_OVP_EN	(Format: binary, access: read/write) Default: 1b Enable fixed output voltage OV protection This bit, when high, enables fixed OV protection circuitry that is active after the BP3 and BP5 voltage comes up. When the bit is low, tracking OV protection is enabled instead and in this case, OV protection is enabled only after the soft-start sequence has completed.
12	DIS_SSPB	(Format: binary, access: read/write) Default: 1b Disable pre-bias initiation after soft-start sequence has completed. This bit affects the PWM signal only during prebias startup. When this bit is high, PWM switching begins only if the COMP voltage is higher than the PWM ramp valley. When this bit is low, PWM switching is forced to begin after soft-start sequence has completed, even when the COMP voltage is lower than PWM ramp valley.

MFR_SPECIFIC_21 (OPTIONS) (E5h)

Format	Unsigned binary
Description	This register is used for setting user selectable options for the controller.
Default	0111 1111 0000 0000 (binary) The default power-up state can be changed using the STORE_USER commands.

Common/Shared							
r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w
7	6	5	4	3	2	1	0
TCO	CH2_CSGAIN_SEL<2:0>		CH1_CSGAIN_SEL<1:0>		en_adc_cntl	EN_TSNS_FLT	EN_SPS

r	r	r	r	r	r	r/w^E	r/w
						SMB_OV	msps_flt

Bits	Field Name	Description
7	TCO	(Format: binary) Default: 0b Temperature compensation override 0: OCF, OCW thresholds and current measurements are temp compensated 1: Temperature compensation is “disabled” TCO is a non-paged bit. Any change on TCO bit is applied to both page 0 and page 1.
6:5	CH2_CSGAIN_SEL<1:0>	(Format: binary) 1:0> Default: 11b Ch2 current-share gain select This 2-bit bus is used to select the gain of the current-sharing circuit in channel 2. For high

		DCR/L ratios, the user can select lower gains for current-loop stability.
4:3	CH1_CSGAIN_SEL<1:0>	(Format: binary) Default: 11b Ch1 current-share gain select This 2-bit bus is used to select the gain of the current-sharing circuit in channel 1. For high DCR/L ratios, the user can select lower gains for current-loop stability. 00: 50 V/V gain 01: 40 V/V gain 10: 30 V/V gain 11: 20 V/V gain
2	en_adc_ctl	(Format: binary) Default: 1b Enable ADC Control Bit. 0: Disable ADC operation. 1: Enable ADC operation.
1	EN_TSNS_FLT	(Format: binary) Default: 1b Enable fault input from Smart power stage This bit, when high, makes the device sensitive to fault communication from the smart power stage. When this bit is low, the device ignores the fault indication from the smart power stage. Whether this bit is high or low, the device performs over temperature protection and declares OT fault when Smart power stage temperature is above the OT fault threshold.
0	EN_SPS	(Format: binary) Default: 1b（forbid change）
7:2		Note: Any values written to read-only registers are ignored.
1	SMB_OV	(Format: binary) Default: 0b Make SMBALERT an OV fault indicator. This has page 0 scope only (in effect, it is defined only on page 0; the page 1 bit is not used). 0: SMBALERT functions normally 1: SMBALERT reports only OV_FAULT
0	msps_flt	(Format: binary) Default: 0b (PAGE scope) 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_MFR_SPECIFIC(3) / STATUS_MFR_SPECIFIC(2) (corresponding to the CH1_SPS_FLT and CH2_SPS_FLT respectively).

MFR_SPECIFIC_22 (PWM_OSC_SELECT) (E6h)

Format	Unsigned binary
Description	This register is used for setting user selectable PWM phase configuration (sync enable, direction of frequency synchronization pulses - in or out - in a master channel and number of phases) in a multi-phase system.
Default	0000h The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
											SYNC_MODE<1:0>		ENSYNC	PHASE	

Bits	Field Name	Description
7:0 7:5		Note: Any values written to read-only registers are ignored.
4:3	SYNC_MODE<1:0>	(Format: binary) Default: 00b Synchronization configuration for the oscillator These bits allow the user to configure the internal PWM oscillator clock in the PWM master channel 1 in one of several operating modes as described below. 1. To change this value, the user must change this value in the register, save it to the EEPROM and then reboot the device via power down for the new value to take effect. 2. If channel 1 is a slave, then these bits are internally forced to <1:1> indicating that external signals on the SYNC and PHDET pins must override the internal clock and phase zero signals. In a case of slave channel 1, any attempt to write a "0" to either one or both bits are treated as invalid data – in effect, the 'cml' bit in the STATUS_BYTE register and the 'ivd' bit in the STATUS_CML register are set, and SMB_ALERT asserted. 00: Self generated clock with internal phasing, switch positions 1 and 3 01: External clock on SYNC pin, but phasing is internal; switch positions 1 and 3 10: External clock on SYNC pin and external phase signal on PHDET pin; switch positions 1 and 3 11: External clock on SYNC pin and external phase signal on PHDET pin; switch positions 2 and 4 (forced for channel 1 slave)
2	ENSYNC	(Format: binary) Default: 0b Synchronization enable This bit, when high, enables the synchronization drivers. 0: Synchronization is disabled 1: Synchronization is enabled

1:0	PHASE	(Format: binary) Default: 00b Number of phases in the system (that involves the IC). This pair of bits is used to configure the number of phases in the power-supply system containing the IC. This information is then used inside the PWM oscillator to set the master switching frequency and channel phase angles. 1. To change this value, the user must change this value in the register, save it to the EEPROM and then reboot the device via power down for the new value to take effect. 2. If channel 1 is a slave, then the bit PHASE <1> is internally forced to 1 indicating that only 3-ph or 4-ph modes can be enabled. In such a case of slave channel 1, any attempt to write a "0" to this bit is treated as invalid data – in effect, the 'cml' bit in the STATUS_BYTE register and the 'ivd' bit in the STATUS_CML register are set, and SMB_ALERT asserted. 00: Independent, dual channel operation 01: Two-phase operation (within single IC) 10: Three-phase operation (between two ICs) 11: Four-phase operation (between two ICs)

NOTE

A 120° phase shift can be achieved between three phases at 3-phase plus 1-phase configuration, the 1-phase rail has the same phase as channel 1 of the master IC.

A 90° phase shift can be achieved between all four phases at all other configurations listed in the table. SYNC pins of two devices need to be connected, and PHSET pins of two devices need to be connected.

Table. Phase Configurations(1)

PHASE CONFIGURATIONS	MASTER IC			SLAVE IC		
	SYNC_MODE	ENSYNC	PHASE	SYNC_MODE	ENSYNC	PHASE
3-phase + 1-phase	00	1	10	11	1	10
4-phase	00	1	11	11	1	11
2-phase + 2-phase	00	(2)	11	11	(2)	11
2-phase + dual-output	00	(2)	11	11	(2)	11
Dual-output + dual-output	00	(2)	11	11	(2)	11

(1) For 3-phase plus 1-phase configuration and 4-phase configuration, SYNC_MODE, ENSYNC and PHASE can be programmed, saved to EEPROM at one time and then reboot the device for the new value to take effect.

(2) For all other configurations listed in the table, follow these steps to program two devices to avoid potential damage.

1. Set ENSYNC to 0 on each device.
2. Program SYNC_MODE and PHASE correctly at both devices, save to the EEPROM and then reboot the devices.
3. Set ENSYNC to 1 on each device to enable synchronization between two devices. No reboot is needed.

MFR_SPECIFIC_23 (MASK SMBALERT) (E7h)

Format	Unsigned binary
Description	The MFR_SPECIFIC_23 (MASK SMBALERT) command may be used to prevent a warning or fault condition from asserting the SMBALERT signal. This command is unique in that it is partially paged; and partially common/shared – since some faults are channel dependent; and others are channel independent. The upper 8 bits of this register always controls and accesses the shared/common set of faults, regardless of the (00h) PAGE setting. However, the control and access for the lower 8 bits of this register are (00h) PAGE dependent and controls or reflects the currently selected page. Only provides below two options for MASK_SMBALERT setting. ● When en_auto_ARA bit (auto Alert Response Address response) is enabled, all other bits in this PMBus register need to be disabled. ● When en_auto_ARA bit is disabled, any other bits in this PMBus register can be set as desired.
Default	0000h The default power-up state can be changed using the STORE_USER commands.

Common/Shared								PAGE0, PAGE1							
r/w	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w	r/w^E	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
motfi	mprtcl_err	msmb_TO_err	mivc	mivd	mpec	mmem	en_auto_ARA	mOTF	mOTW	mOCF	mOCW	mOVF	mUVF	mPGOOD_Z	mVIN_UV

Bits	Field Name	Description
7	motfi	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_MFR_SPECIFIC(7)
6	mprtcl_err	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of SMB Protocol Error from the PMBus interface module. One of 2 sources is STATUS_CML(1).
5	msmb_TO_err	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of SMB_TIMEOUT from the PMBus interface module. One of 2 sources is STATUS_CML(1).
4	mivc	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_CML(7)
3	mivd	(Format: binary)

		Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_CML(6)
2	mpec	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_CML(5)
1	mmem	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_CML(4)
0	en_auto_ARA	(Format: binary) Default: 0b Enables auto Alert Response Address response. When this feature is enabled, the hardware automatically masks any fault source currently set from re-asserting SMB_ALERT when this device responds to an ARA on the PMBus. This prevents PMBus "bus hogging" in the case of a persistent fault in a device that consistently wins ARA arbitration due to its device address. In contrast, when this bit is cleared, immediate re-assertion of SMB_ALERT is allowed in the event of a persistent fault and the responsibility is upon the host to mask each source individually. When WRITE_PROTECT is set to 20h, 40h or 80h, en_auto_ARA is enabled automatically.
7	mOTF	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_TEMPERATURE(7)
6	mOTW	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_TEMPERATURE(6)
5	mOCF	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_IOUT(7)
4	mOCW	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_IOUT(5)
3	mOVF	Functionality of mask bit: (Format: binary)

		Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_VOUT(7)
2	mUVF	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_VOUT(4)
1	mPGOOD_Z	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_WORD(11)
0	mVIN_UV	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_BYTE(3)

MFR_SPECIFIC_30 (TEMP_OFFSET) (EFh)

Format	Unsigned binary
Description	This paged register is used for setting user selectable offset in the measured temperature. The specified offset value is added to the post-math digital output. The new, post-offset, post-averaging temperature is used for READ_TEMP_2 reporting and for temperature compensation of IOUT_CAL_GAIN for both reporting READ_IOUT, and OC_FAULT_LIMIT/WARN threshold setting.
Default	F800h The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r/w^E	r	r	r	r	r	r	r	r/w^E	r/w^E	r
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's complement) This is the exponent for the linear format. Default: 11111 (bin) –1 (dec) (LSB = 0.5 deg) These default settings are not programmable.
2:0 7:0	Mantissa	(Format: two's complement) Default: 000 (bin) 0 (dec) (0 deg) Minimum 7F8 = –8 x 0.5 deg = –4 deg Maximum 006 = 6 x 0.5 deg = 3 deg

MFR_SPECIFIC_44 (DEVICE_CODE) (FCh)

Format	Unsigned binary
Description	The DEVICE_CODE command returns a 12-bit unique identifier code for the device and a 4-bit device revision code.
Default	01E0h

r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Bits	Field Name	Description
7:0 7:4	Identifier Code	0000 0001 1110b : Device ID Code Identifier for the device
3:0	Revision Code	0000b : Revision Code (first silicon starts at 0)

注：

1. 包装信息请参见《产品出货包装信息》，载带卷盘包装包编号：58210321；
2. 最大容性负载均在输入电压范围、满负载条件下测试；
3. 除特殊说明外，本手册所有指标都在 Ta=25℃，湿度<75%RH，标称输入电压和正输出额定负载时测得；
4. 本手册所有指标的测试方法均依据本公司企业标准；
5. 我司可提供产品定制，具体需求可直接联系我司技术人员；
6. 产品涉及法律法规：见“产品特点”；
7. 我司产品报废后需按照 ISO14001 及相关环境法律法规分类存放，并交由有资质的单位处理。

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